Priyank Kalla

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Professional Experience

- **Professor** (July 2018 - present). Department of Electrical and Computer Engineering, University of Utah. Areas of Expertise: Formal hardware verification and Electronic design automation. Was Associate Professor (2009-2018), and Assistant Professor (2002-2009).
- **Visiting Professor**, VLSI Design and Education Center, The University of Tokyo, May - Aug 2018.
- **Visiting faculty**, Department of Electrical and Computer Engineering, University of Massachusetts at Amherst, Amherst MA, January - May 2017.
- **Visiting Professor**, Informatik Dept., University of Bremen, Germany, March - July 2010.
- **Product Development Engineer**, **Compaq Corp.**, Shrewsbury, MA, USA (May 2000 - February 2001). Worked with **Alpha Microprocessor CAD and Test Group**.
- **Product Development Engineer**, **Cadence Design Systems**, Chelmsford, MA, USA (June 1996 - August 1996). Worked with the **Logic Synthesis** group.
- **Product Development Engineer**, **Advanced Micro Devices**, Austin, TX, USA (August 1995 - January 1996). Worked with **K-7 Microprocessor group**.
- **Product Development Engineer**, **Amtel Research**, Baroda, India (October 1993 - June 1994). Was involved in developing a micro-controller and PC-based card activated system controlling access to facilities.

Academic Record

- **Ph.D.** Electrical & Computer Engineering (Degree Received: Sept. 2002)
  University of Massachusetts at Amherst, MA, USA
  Dissertation: An Infrastructure for RTL Validation and Verification
  Advisor: Professor Maciej Ciesielski
- **M.S.** Electrical & Computer Engineering (Degree Received: May 1998)
  University of Massachusetts at Amherst, MA, USA
  Thesis: Testability of Sequential Circuits with Multi-Cycle False Paths
  Advisor: Professor Maciej Ciesielski
- **B.E.** Electronics Engineering (Degree Received: October 1993)
  Birla Vishvakarma Mahavidyalaya
  Sardar Patel University, Vallabh Vidyanagar, Gujarat, India
  Graduated in First Class with Distinction

Honours and Awards

Research and Scholarship Awards

- **Honourable Mention Paper Award**, International Test Conference India, 2022. Awarded for the paper:
  Pratishtha Agnihotri, Priyank Kalla and Steve Blair, *"Transfer-Matrix Abstractions for to Analyze the Effect of Manufacturing Variations in Silicon Photonic Circuits"*, IEEE Intl. Test Conf. India (ITC India), pp. 1-8, July 2022.
- **Best Paper with Student as First Author Award:** International Workshop on Logic and Synthesis (IWLS) 2017, for the paper:
  - *Boolean Gröbner Basis Reductions on Datapath Circuits using the Unate Cube Set Algebra*, **Utkarsh Gupta**, Priyank Kalla and Vikas Rao, IWLS 2017, pp. 124-131.
- **Best Paper with Student as First Author Award:** IEEE Mid-West Symposium on Circuits and Systems (MWSCAS) 2013, for the paper:
  - *Crossing-Aware Channel Routing for Photonic Waveguides*, **Christopher Condrat**, Priyank Kalla and Steve Blair, IEEE MWSCAS 2013, pp. 649-652.
- **Bronze Medal:** ACM Student Research Competition for the undergraduate thesis of my student Lawrence Schlitt, *Effects of Thermal Stress on Silicon Photonic Waveguide Operation*. Award given at the Design Automation Conference (DAC) 2012.
- **Best Paper Award:** ACM Transactions on Design Automation of Electronic Systems (TODAES) 2009, for the paper:
  - *Optimization of polynomial datapaths using finite ring algebra*, Sivaram Gopalakrishnan and Priyank Kalla, ACM Trans. Design Automation (TODAES), vol 12, issue 4, article 49, Sept. 2007.
- US National Science Foundation, Faculty Early Career Development (**CAREER**) Award, 2006. Awarded research grant amount: **$401,967.** Grant duration Feb 2006 - Jan 2012.

Teaching Awards

- **Outstanding Teacher** awarded by Computer Engineering graduating class of 2020.
- Dean's acknowledgment for being placed among the **top 15% instructors** in the College of Engineering, Univ. of Utah, based on student evaluations:
  - Fall 2015 and 2007, for the undergraduate course ECE/CS 3710: Computer Design Lab.
  - Fall 2008, for the graduate course ECE/CS 5745/6745: Testing and Verification of Digital Circuits.
- **Outstanding Teaching Assistant Award:** Received for assisting in the organization, management and laboratory instruction for the freshman course "Introduction to Engineering," College of Engineering, University of Massachusetts at Amherst, Fall 1996.

Service Awards

- **Outstanding Service Award:** ECE Department, Univ. of Utah, AY 2021.

Best Paper Nominations

- Best Paper Award Nomination: IEEE/IFIP Intl. Conf. on VLSI (VLSI-SoC), 2018, for the paper:
  - *On the Rectifiability of Arithmetic Circuits using Craig Interpolants in Finite Fields*, U. Gupta, I. Ilioaea, V. Rao, A. Srinath, P. Kalla and F. Enescu. Paper presentation and award decision in October 2018.
- Best Paper Award Nomination: IEEE Transactions on Computer-Aided Design (IEEE TCAD) 2014, for the paper:
  - *Efficient Gröbner Basis Reductions for Formal Verification of Galois Field Arithmetic Circuits*, Jinpeng Lv, **Priyank Kalla** and Florian Enescu, IEEE Trans. on CAD, vol. 32, issue 9, pp. 1409 - 1420, Sept. 2013.
- **Best Paper Award Nomination:** IEEE/ACM Design Automation and Test in Europe (DATE) Conf. 2001, for the paper:
  - Zhihong Zeng, **Priyank Kalla** and Maciej Ciesielski, "LPSAT: A Unified Approach to RTL-Satisfiability," in *Proc. IEEE/ACM Design, Automation and Test in Europe* Conf., (DATE), pp. 398-402, March 2001.

Teaching Experience & Responsibilities

- **Hardware Cryptography and Security**. New course introduced as a special topics in Spring 2022.
- **Hardware Verification using Algebraic Geometry and Symbolic Computation**. Fall '14, '17. A new graduate course that covers formal hardware datapath verification using techniques from computational commutative algebra and algebraic geometry. I developed and introduced this course in 2014 based on my research experience in this area.
- **Testing and Verification of Digital Circuits**, Fall '12, '08, '06, '04, '02. Graduate course in VLSI Testing, Logic Validation and Equivalence Verification. Electrical and Computer Engineering, University of Utah. I introduced this course in the ECE/CS curriculum in 2002.
- **Computer-Aided Design of Digital Circuits**, Spring '16, '14, '12, '08, '06, '04. A graduate course in automated Synthesis and Optimization of digital circuits and systems. Covers topics in Logic and behavioural synthesis. In Spring '14, this course was taught as *VLSI Physical Design Automation*, covering topics in VLSI floor-planning, placement, routing and physical synthesis.
- **Computer Algebra for Electrical & Computer Engineers**, Summer semester 2010, Informatik Department, University of Bremen, Germany. Taught this as a pilot course while on sabbatical at the Univ. of Bremen. Course covered Gröbner Bases, Galois Fields and Polynomial Function theory for Engineering applications.
- **Fundamentals of Digital System Design**, Spring '15,'13, '11, '09, '07, '05, '03. Introductory digital logic design course for undergraduate students in ECE and CS Depts., University of Utah.
- **Digital Computer Design Laboratory**, Fall '15, '13, '11, '07, '05, '03. A laboratory oriented course as a follow-up to the introductory digital logic design. Students design a 16-bit computer, interface it with IO peripherals and build their own applications. ECE and CS Depts., University of Utah.
- **Senior Capstone Project Supervision:** Every year 2002-2014. Team projects sponsored by local industry in Utah.

Research Interests and Projects

- Formal hardware verification using computational commutative algebra and algebraic geometry.
  - Modeling of datapath designs as polynomial functions over finite fields and finite integer rings.
  - Application of finite ring algebra for RTL synthesis and verification of arithmetic datapaths.
  - Formal verification and design abstraction at the word-level using algebraic geometry.
  - Word-level Craig's interpolants and unsatisfiable cores in algebraic geometry.
  - Gröbner bases for symbolic reasoning and abstraction in design validation.
- New directions in symbolic computer algebra algorithms using logic synthesis techniques.
  - Boolean Gröbner bases as a Boolean function decomposition problem.
  - Polynomial computations as the unate cube-set algebra.
- Design automation and Test for Silicon-based integrated optics (Si-photonics).
  - Design for Testability and Debug for Silicon-photonics.
  - Synthesis of thermal-reliable and manufacturability-aware nanophotonic integration.
  - Logic synthesis for integrated optics.
  - Thermal-aware synthesis of integrated photonic resonators and interferometers.
  - Physical design automation for integrated optical devices and photonic waveguides.
- Security modeling and detection in integrated circuits.
- Integration of hybrid constraint satisfaction engines.

Professional Service Activities

- Technical Program Co-Chair, Intl. Test Conference India (ITC-India), 2023.
- Technical Committee Chair for EDA Track, Intl. Conf. on Computer Design (ICCD), 2020, 2021 conferences.
- Technical Program Committee Member, Intl. Conf. CAD, 2021, 2022.
- *Associate Editor*, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), 2016-present.
- *Chair*, IEEE Circuits and Systems Society (CASS) Technical Committee on Computer-Aided Network Design (CANDE) 2011-2012. Served as *Past Chair* 2012-2014.
- *General Chair*, IEEE International High-Level Design Validation and Test Workshop, HLDVT 2009. Was the *Technical Program Chair* for HLDVT 2008, and *Finance Chair* HLDVT 2007.
- *Member*, Technical Program Committee of various conferences and workshops: Intl. Conf. on CAD (ICCAD 5 yrs), Intl. Conf. Computer Design (ICCD 2 yrs), Constraints in Formal Verification (CFV 2 yrs), Design & Implementation of Formal Tools and Systems (DIFTS 3 yrs), IEEE HLDVT (5 yrs), etc.
- *Reviewer*, Grant proposals, US National Science Foundation, 2005, 2007, 2013, 2015.
- *Reviewer*, Technical papers, Design Automation Conference, Design Automation and Test in Europe Conference, IEEE Transactions on Computers, IEEE Transactions on Computer-Aided Design, ACM Transactions on Design Automation of Electronic Systems, IEE Proc. Computers and Digital Design Techniques, among other journals and conferences.

Academic Service Activities

- *Chair, Undergraduate College Curriculum Committee*, Fall 2021 - present.
- *ABET Coordinator* for the ECE/SoC Computer Engineering Program, 2018 - 2021.
- *Director, Computer Engineering Program*, Dept. of ECE, Univ. of Utah, Aug 2018 - 2021.
- *Director of Graduate Programs*, Dept. of Electrical and Computer Engineering, Univ. of Utah, 2013 - 2018.
- *Member*, University of Utah Student Computing Advisory Committee. 2011 - present.
- *Member*, ECE Dept. Marketing Committee, Univ. of Utah, 2011-present.
- *Member*, Computer Engineering Program Committee, Dept. of Electrical and Computer Engineering, Univ. of Utah, 2002-2006.
- *Member*, Graduate program committee, 2002-2013.
- *Secretary*, College of Engineering Council, 2002-2009.

Graduate Student Supervision

- **Vikas Rao:** PhD completed Summer 2021. Currently employed as Sr. Member R&D (Formal Verification) Synopsys, Inc., Portland, OR.
  - PhD Dissertation: *Rectification of Arithmetic Circuits with Computer Algebra Techniques*.
- **Utkarsh Gupta:** PhD completed Spring 2020. Currently employed as Formal Verification Engineer, Apple Inc., Portland, OR.
  - PhD Dissertation: *Rectification of Finite Field Arithmetic Circuits with Craig Interpolation using Algebraic Geometry*.
- **Arpitha Srinath:** M.S. thesis defended Sept. 2019. Currently employed as Test Engineer, Micron.
- **Xiaojun Sun:** PhD completed December 2016. Currently employed as Lead Software Engineer, Cadence Design Systems, San Jose, CA.
  - PhD Dissertation: *Word-Level Abstractions for Sequential Design Verification using Algebraic Geometry*.
- **Tim Pruss:** PhD completed Summer 2015. Currently, Formal Verification Engineer, Apple Inc., Cupertino, CA.
  - PhD Dissertation: *Word-Level Abstraction from Combinational Circuits using Algebraic Geometry*.
- **Christopher Condrat:** PhD Fall 2013, combined BS/MS Fall 2007. Currently, Lead Member Technical Staff, Calypto product group of Mentor Graphics, Portland, OR.
  - PhD Dissertation: *Design Automation for Integrated Optics*.
- **Jinpeng Lv:** PhD completed Fall 2012. Currently, Senior software development engineer, Microsoft Corp., Seattle, WA.

  - PhD Dissertation: *Scalable Formal Verification of Finite Field Arithmetic Circuits using Computer Algebra Techniques*.

- **Sivaram Gopalakrishnan:** PhD Aug 2008; MS May 2004. Currently, Senior R & D Engineer II, Formality Group, Synopsys Inc., Portland, OR.
  - PhD Dissertation: *RTL Synthesis of Polynomial Datapaths using Finite Integer Algebras*.
- **Namrata Shekhar:** PhD, Fall 2007. Currently, Senior R & D Engineer, Formality Group, Synopsys Inc., Marlboro, MA.
  - PhD Dissertation: *Equivalence Verification of Arithmetic Datapaths using Finite Ring Algebra*.
- **Vijay Durairaj:** MS 2004. Currently, Senior R & D Engineer, ESP Group, Synopsys Inc., Santa Clara, CA.
- **Lawrence Schlitt:** Current PhD student, BS/MS Fall 2014.
- **Pratishtha Agnihotri:** PhD student started Spring 2021.
- **Bhavani Sampathkumar:** PhD Student started Spring 2022.
- **Ritaja Das:** PhD Student started Spring 2022.
- **Bailey Martin:** BS/MS Student.

Funding for our Research

- *Collaborative Proposal: Partial Logic Synthesis*. Submitted to the U.S. National Science Foundation. Proposal Budget: $386,251.
  Co-PI: Florian Enescu, Math & Stats, Georgia State Univ. Proposal status: **pending**.
- *Collaborative Proposal: Rectification of Arithmetic Circuits with Craig Interpolation in Algebraic Geometry*. Funded by NSF 2019-2023. Award amount: **$309,905**.
- *New Directions in Gröbner Basis based Verification using Logic Synthesis Techniques*. Funded by Computer and Communication Foundation Core Program, National Science Foundation, 2016-2019. Award Amount: **$390,999.**
- *Efficient Computer Algebra Techniques for Scalable Verification of Galois Field Arithmetic Circuits*. Funded by Computer and Communication Foundation Core Program, National Science Foundation, 2013-2016. Award Amount: **$393,312.** Collaborative Proposal with Prof. Florian Enescu, Georgia State University.
- *Ensuring Trust in Pre-Silicon Hardware IPs*. Univ. of Utah Research Foundation SEED Grant Program, 2013-2014. Award Amount: **$23,310.**
- *Optical Logic Design*. Was Co-PI on this AFOSR sub-contract from Fisk University. PI: Steven Blair. Total amount: **$50,000** May 2010 - June 2013.
- *GOALI: Word-Level Techniques for Verification of Bit-Vector Arithmetic*. US National Science Foundation, CISE Directorate. Total amount: **$80,379**. Awarded as **Grant Opportunities for Academic Liaison with Industry (GOALI)** supplement to CAREER award. Industry Partner: Calypto Design Systems, Santa Clara, USA. Duration: August 2008 - Jan 2011.

- *CAREER: Exploring Symbolic Algebra for RTL Verification of Arithmetic Datapaths*. US National Science Foundation, CISE Directorate. Awarded as **Faculty Early Career (CAREER) Development Award**. Total amount: **$401,967**. Feb 2006 - Jan 2011. Jointly awarded by the Symbolic Computing Program and the Design Automation Program.

- *Collaborative Research: A New Theoretical and Algorithmic Framework for RTL Datapath Verification using Polynomial Algebra over Finite Integer Rings*. US National Science Foundation. Symbolic Computing Program, CISE Directorate. Award amount **$75,000**, July 2005 - June 2006. Co-investigator: Prof. Florian Enescu, Mathematics & Statistics, Georgia State Univ., USA.

- *Exploring Symbolic Computer Algebra for High-Level Datapath Verification*. Univ. of Utah Research foundation, SEED grant. May 2005 - Dec 2005. Award amount: **$17,000.**

Books and Book Chapters Published

- **Priyank Kalla**, *"Hardware Verification using Algebraic Geometry"*, a textbook under preparation describing symbolic computer algebra and algebraic geometry techniques for formal hardware verification. The book will be self published. The partially completed chapters are already made available in public domain at `http://www.ece.utah.edu/~kalla/book.pdf`.

- Utkarsh Gupta, Irina Ilioaea, Vikas Rao, Arpitha Srinath, **Priyank Kalla**, and Florian Enescu, "Rectification of Arithmetic Circuits with Craig Interpolation in Finite Fields", **invited chapter** in book *VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms*, Eds. N. Bombieri et al., Springer, pp. 79-106, 2019.

- Robert Wille, Krishnendu Chakrabarty, Rolf Drechsler, and **Priyank Kalla**, "Emerging Circuit Technologies: An Overview on the Next Generation of Circuits", **invited chapter** in book on *Selected Contributions in Logic Synthesis*, Eds. Rolf Drechsler and André Reis, Springer, pp. 43-68, 2018.

- Christopher Condrat, **Priyank Kalla** and Steve Blair, "Design Automation for On-Chip Nano-Photonic Integration," **invited chapter** in book *"More than Moore Technologies for Next Generation Computer Design"*, Springer-New York, 2015. Chapter 8, pp. 187-218. Editor: Rasit O. Topaloglu.

- Sivaram Gopalakrishnan and **Priyank Kalla**, "Algebraic Techniques to Enhance Common Sub-Expression Extraction in Polynomial System Synthesis", **invited chapter** in book *Advances in Logic Synthesis, Optimization and Applications*, Springer-New York, 2011. Editors: K. Gulati and S. Khatri.

- **Priyank Kalla** and Maciej Ciesielski, "Logic Testing," **invited article** in *Wiley Encyclopedia of Electrical and Electronics Engineering*, John Wiley and Sons, Inc., Ed. John G. Webster, vol. 11, pp. 591-597, 1999.

Refereed Journal Publications

- Xiaojun Sun, **Priyank Kalla** and Florian Enescu, "Word-Level Reachability Analysis of Finite State Machines using Algebraic Geometry Techniques", currently under review in *ACM Trans. on Design Automation of Electronic Systems*.

- Utkarsh Gupta, **Priyank Kalla**, Vikas Rao, "Efficient Boolean Gröbner Basis Reductions on Datapath Circuits using the Unate Cube Set Algebra," in *IEEE Trans. on CAD*, vol 38, issue 3, pp. 576-588, March 2019.

- Tim Pruss, **Priyank Kalla** and Florian Enescu, "Efficient Symbolic Computation for Word-Level Abstraction from Combinational Circuits for Verification over Finite Fields", in *IEEE Trans. CAD*, vol. 35, no. 7, pp. 1206-1218, July 2016.

- Christopher Condrat, **Priyank Kalla**, Steve Blair, "Crossing-Aware Channel Routing for Integrated Optics", IEEE Transactions on CAD, special issue on *Optical Interconnects*, June 2014, vol. 33, issue 9, pp. 814-825.

- Jinpeng Lv, **Priyank Kalla** and Florian Enescu, "Efficient Gröbner Basis Reductions for Formal Verification of Galois Field Arithmetic Circuits", IEEE Trans. on CAD, vol. 32, issue 9, pp. 1409 - 1420, Sept. 2013.

  - **Nominated for 2014 Best Paper Award**

- Namrata Shekhar, **Priyank Kalla**, M. Brandon Meredith and Florian Enescu. "Simulation Bounds for Equivalence Verification of Arithmetic Datapaths using Finite Ring Algebra," in *IEEE Trans. on VLSI*, special section on Design Validation and Verification, pp. 376-387, vol. 16, issue 4, April 2008.

- Sivaram Gopalakrishnan and **Priyank Kalla**, "Optimization of Polynomial Datapaths using Finite Ring Algebra," in *ACM Trans. on Design Automation* (ACM-TODAES), vol 12, issue 4, article 49, September 2007.

  - Received the 2009 ACM TODAES **Best Paper Award**.

- Namrata Shekhar, **Priyank Kalla** and Florian Enescu. "Equivalence Verification of Arithmetic Datapaths using Ideal Membership Testing," in *IEEE Trans. on CAD*, pp. 1320-1330, vol. 26, number 7, July 2007.

- Maciej Ciesielski, **Priyank Kalla**, and Serkan Askar. "Taylor Expansion Diagrams: A Canonical Representation for Verification of Data Flow Designs," in *IEEE Transactions on Computers*, vol. 55, no. 9, pp. 1188-1201, Sept. 2006.

- Navin Vemuri, **Priyank Kalla** and Russell Tessier, "BDD-Based Logic Synthesis for LUT-Based FPGAs," in *The ACM Transactions on Design Automation, special issue on Programmable Logic*, vol. 7, no. 4, pp 501-525, Oct 2002.

- **Priyank Kalla** and Maciej Ciesielski, "A Comprehensive Approach to the Partial Scan Problem using Implicit State Enumeration," in *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 21, no. 7, July 2002.

- **Priyank Kalla**, Zhihong Zeng and Maciej Ciesielski, "Strategies for Solving the Boolean Satisfiability Problem using Binary Decision Diagrams," in *Journal of Systems Architecture, The Euromicro Journal*, vol. 47/6, pp. 491-503, September 2001.

Refereed Conference Publications

- Bhavani Sampathkumar, Bailey Martin, Ritaja Das, **Priyank Kalla** and Florian Enescu, "Logic Synthesis from Polynomials with Coefficients in the Field of Rationals", accepted, to appear in Proc. *IEEE International Symposium on Multi-Valued Logic*, May 2023.

- Pratishtha Agnihotri, **Priyank Kalla**, Steve Blair, "Transfer-Matrix Abstractions to Analyze the Effect of Manufacturing Variations in Silicon Photonic Circuits", in Prof. *IEEE Intl. Test Conference India (ITC India)*, pp. 1-8, 2022, doi: 10.1109/ITCIndia202255192.2022.9854738.

  - **Honourable Mention Paper Award**.
  - The same publication was also **invited** for a presentation at the International Test Conference in USA 2022.

- Vikas Rao, Haden Ondricek, **Priyank Kalla** and Florian Enescu. "Rectification of Integer Arithmetic Circuits using Computer Algebra Techniques", in Proc. Intl. Conf. on Computer Design (ICCD), Oct 2021.
- Vikas Rao, Haden Ondricek, **Priyank Kalla** and Florian Enescu. "Algebraic Techniques for Rectification of Finite Field Circuits", in Proc. Intl. Conf. on VLSI (VLSI SoC), Oct 2021.
- Vikas Rao, Haden Ondricek, **Priyank Kalla** and Florian Enescu. "On the Rectification of Finite Field Arithmetic Circuits using Computer Algebra Techniques", in Proc. Intl. Workshop on Logic and Synthesis (IWLS), June 2021.
- Vikas Rao, Irina Ilioaea, Haden Ondricek, **Priyank Kalla** and Florian Enescu. Word-Level Multi-Fix Rectifiability of Finite Field Arithmetic Circuits, in Proc. Intl. Symp. on Quality Electronic Design (ISQED), 2021.
- Utkarsh Gupta, **Priyank Kalla**, Irina Ilioaea, and Florian Enescu. "Exploring Algebraic Interpolants for Rectification of Finite Field Arithmetic Circuits using Gröbner Bases," in Proc. European Test Symposium, 2019.
- Vikas Rao, Utkarsh Gupta, Irina Ilioaea, Arpitha Srinath, **Priyank Kalla** and Florian Enescu. "Post-Verification Debugging and Rectification of Finite Field Arithmetic Circuits using Computer Algebra Techniques," in Proc. *Formal Methods in Computer-Aided Design (FMCAD)*, Nov. 2018.
- Utkarsh Gupta, Irina Ilioaea, Vikas Rao, Arpitha Srinath, **Priyank Kalla** and Florian Enescu. "On the Rectifiability of Arithmetic Circuits using Craig Interpolants in Finite Fields," in Proc. *IFIP/IEEE/AICA Intl. Conf. in VLSI (VLSI-SoC)*, October 2018.
  - *Best paper award nomination.*
- Utkarsh Gupta, Irina Ilioaea, **Priyank Kalla** and Florian Enescu, Vikas Rao and Arpitha Srinath. "Craig Interpolants in Finite Fields using Algebraic Geometry: Theory and Application", in Proc. *Intl. Workshop on Logic and Synthesis (IWLS)*, 2018.
- Vikas Rao, Utkarsh Gupta, Irina Ilioaea, **Priyank Kalla** and Florian Enescu. "Resolving Unknown Components in Arithmetic Circuits using Computer Algebra Methods", in Proc. *Intl. Workshop on Logic and Synthesis (IWLS)*, 2018.
- Utkarsh Gupta, Irina Ilioaea, **Priyank Kalla** and Florian Enescu. "Craig Interpolants in Finite Fields using Algebraic Geometry: Theory and Algorithms", in review Proc. *Intl. Joint Conferences on Automated Reasoning*, 2018.
- Utkarsh Gupta, **Priyank Kalla**, Vikas Rao, "Boolean Gröbner Basis Reductions on Datapath Circuits using the Unate Cube Set Algebra," in Proc. *Intl. Workshop on Logic and Synthesi (IWLS)*, pp. 124-131, 2017.
  - **Best paper with student as first author award.**
- Xiaojun Sun, **Priyank Kalla** and Florian Enescu, "Word-Level Traversal of Finite State Machines using Algebraic Geometry", in Proc. *Intl. Workshop on High-Level Design Validation and Test,* HLDVT 2016, pp. 142-149.
- Xiaojun Sun, Irina Ilioaea, **Priyank Kalla** and Florian Enescu. "Finding Unsatisfiable Cores of a Set of Polynomials using The Gröbner Basis Algorithm", in Proc. *Intl. Conf. Principles and Practise of Constraint Programming*, pp. 859-875, LNCS vol. 9892, CP 2016.
- Lawrence Schiltt, **Priyank Kalla** and Steve Blair, "A Methodology for Thermal Characterization Abstraction for Integrated Opto-Electronic Layouts", in Proc. *Intl. Conf. VLSI Design*, pp. 270-275, Jan 2016.

- M. Potkonjak, D. Chen, **P. Kalla** and S. Levitan, "DA Vision: From Here to Eternity", invited paper in special session, *IEEE/ACM Intl. Conf. CAD*, (ICCAD), pp. 271-277, 2015.

- **Priyank Kalla**, "Formal Verification of Arithmetic Datapaths using Algebraic Geometry and Symbolic Computation", **invited tutorial paper**, in *Proc. Formal Methods in CAD (FMCAD)*, pp. 2-2, 2015. Tutorial presented at the joint session of FMCAD and SAT conferences and the DIFTS workshop.

- Xiaojun Sun, **Priyank Kalla** and Florian Enescu, "Formal Verification of Sequential Galois Field Arithmetic Circuits using Algebraic Geometry", in Proc. *Design Automation & Test in Europe* (DATE) Conf., pp. 1623-1628, March 2015.

- Christopher Condrat, **Priyank Kalla** and Steve Blair, "Thermal-Aware Synthesis of Integrated Photonic Ring-Resonators", in Proc. *Intl. Conf. on Computer-Aided Design (ICCAD)*, pp. 557-564, 2014.

- Tim Pruss, **Priyank Kalla** and Florian Enescu, "Equivalence Verification of Large Galois Field Arithmetic Circuits using Word-Level Abstraction via Groebner Bases", in Proc. *IEEE/ACM Design Automation Conference* (DAC), pp. 1-6, 2014.

- Christopher Condrat, **Priyank Kalla** and Steve Blair, "Crossing-Aware Channel routing for Photonic Waveguides", IEEE *Mid-West Symposium on Circuits and Systems* (MWSCAS), pp. 649-652, Aug 2013.

  - **Winner Best Paper Award with Student as First Author.**

- Tim Pruss, **Priyank Kalla** and Florian Enescu, "Word-Level Abstraction from Bit-Level Circuits using Gröbner Bases", in *Intl. Workshop on Logic and Synthesis* (IWLS), 2013.

- Christopher Condrat, **Priyank Kalla** and Steve Blair, "Channel routing for Integrated Optics", IEEE/ACM *Intl. System-Level Interconnect Prediction Workshop* (SLIP), pages 1-8, 2013, DOI: 10.1109/SLIP.2013.6681678.

- Christopher Condrat, **Priyank Kalla** and Steve Blair, "A Methodology for Physical Design Automation for Integrated Optics", *IEEE MidWest Symposium on Circuits and Systems* (MWSCAS), pp. 598 - 601, 2012.

  - **Invited Paper in special session.**

- Jinpeng Lv, **Priyank Kalla**, and Florian Enescu, "Efficient Groebner Basis Reductions for Formal Verification of Galois Field Multipliers", IEEE/ACM *Design Automation and Test in Europe* (DATE) Conf., pp. 899-904, 2012. Acceptance rate: 26%.

- Jinpeng Lv and **Priyank Kalla**, "Formal Verification of Galois Field Multipliers using Computer Algebra Techniques," IEEE *Intl. Conf. on VLSI Design*, India, pp. 388-393, 2012. Acceptance rate: 30%.

- Jinpeng Lv, **Priyank Kalla** and Florian Enescu, "Verification of Composite Galois Field Multipliers over $GF((2^m)^n)$ using Computer Algebra Techniques", IEEE *Intl. High-Level Design Validation and Test Workshop*, HLDVT, pp. 136-143, Nov 2011.

- Chris Condrat, **Priyank Kalla**, and Steven Blair, "Logic Synthesis for Integrated Optics", in Proc. *ACM Great Lakes Symposium on VLSI*, GLS-VLSI, pp. 13- 18, 2011. Acceptance rate: 26%.

- Chris Condrat, **Priyank Kalla**, and Steven Blair, "Exploring Design and Synthesis for Optical Digital Logic", in Proc. *Intl. Workshop on Logic and Synthesis*, IWLS, 2010, pp. 47 - 54.

- Sivaram Gopalakrishnan and **Priyank Kalla**, "Algebraic Techniques to Enhance Common Sub-Expression Extraction for Polynomial System Synthesis", in Proc. IEEE/ACM *Design Automation and Test in Europe Conf.*, pp. 1452-1457, DATE 2009.

- Neal Tew, **Priyank Kalla**, Namrata Shekhar, Sivaram Gopalakrishnan, "Verification of Arithmetic Datapaths using Polynomial Function Models and Congruence Solving", in Proc. *IEEE/ACM Intl. Conf. on Computer-Aided Design (ICCAD)*, pp. 122-128, Nov. 2008. Acceptance rate: 122/458 = 26.6%.

- **Priyank Kalla**, Neal Tew, Namrata Shekhar, Sivaram Gopalakrishnan, "RTL Verification of Arithmetic Datapaths using Finite Integer Algebras", presented at the *First International Workshop on Bit-Precise Reasoning* (BPR'08), July 2008.

- Sivaram Gopalakrishnan, **Priyank Kalla**, "Integrating Common Sub-expression Elimination with Algebraic Methods for Polynomial System Synthesis" in *Proc. International Workshop on Logic and Synthesis*, (IWLS), pp. 31-37, June 2008.

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- **Priyank Kalla**, Zhihong Zeng, Maciej Ciesielski and Chilai Huang, "A BDD-Based Satisfiability Infrastructure using the Unate Recursive Paradigm," in *Proc. IEEE/ACM Design, Automation and Test in Europe*, (DATE), pp. 232-236, April 2000.

- **Priyank Kalla** and Maciej Ciesielski, "Performance Driven Resynthesis by Exploiting Retiming-Induced State Register Equivalence," in *Proc. IEEE/ACM Design, Automation and Test in Europe*, DATE'99, pp. 638-642, March 1999.

- **Priyank Kalla** and Maciej Ciesielski, "A Comprehensive Approach to the Partial Scan Problem using Implicit State Enumeration," in *Proc. IEEE International Test Conference*, ITC'98, pp. 651-657, October 1998.

- Surendra Bommu, Maciej Ciesielski, Niall O'Neill, and **Priyank Kalla**, "Sequential Logic Optimization with Implicit Retiming and Resynthesis," in *Proc. IFIP International Conference on VLSI*, VLSI'97, pp. 327-338, August 1997.

- **Priyank Kalla** and Maciej Ciesielski, "Testability of Sequential Circuits with Multi-Cycle False Paths," in *Proc. IEEE VLSI Test Symposium*, VTS'97, pp. 322-328, April 1997.

Invited Keynote, Tutorials and Seminars

- Invited Tutorial, "Design and Automation for Silicon Photonic Integration", at the 2021 Test Summer School, May 2021, organized as part of the European Test Symposium, 2021.

- Invited Talk, "Design Automation for Silicon Nanophotonic Integration," at the 14th Design to Test (D2T) Symposium, University of Tokyo, Sept. 2019.
- Invited Tutorial, "Word-Level Abstractions for Datapath Designs using Algebraic Geometry", given at the IEEE High-Level Design Validation and Test Workshop, HLDVT, Oct 2016.
- Keynote Talk, "What can Algebraic Geometry tell us about the Function Implemented by a Circuit?", delivered at the 3rd Workshop on Design Automation for Understanding Hardware Design (DUHDe), 2016.
- Colloqium Seminar, "Word-Level Abstractions from Digital Circuits using Algebraic Geometry and Symbolic Computation", delivered at the Informatik-Kolloquium, Johannes Kepler Univ., Linz, Austria, March 2016.
- Invited Tutorial, "Formal Verification of Arithmetic Datapaths using Algebraic Geometry and Symbolic Computation", given at the joint session of FMCAD, SAT and the DIFTS conferences, Sept. 2015.
- Invited Tutorial, "Leveraging Gröbner Bases and SAT for Hardware/Software Verification", at the Banff International Research Station workshop on Theoretical Foundations of Applied SAT Solving, Jan 2014.
- Colloquium Seminar, "Formal Verification of Galois Field Arithmetic Circuits using Computer Algebra Techniques", delivered at IBM T. J. Watson Research Center, Jan 2013.
- Invited Paper, "A Methodology for Physical Design Automation for Integrated Optics", at IEEE MidWest Symp. on Circuits and Systems, Aug 2012.
- Colloquium Seminar, "Verification of Finite-Precision (Bit-Vector) Arithmetic using Finite Integer Algebras", delivered at the University of Bremen, June 2009, Bremen, Germany.
- Keynote Seminar, "Verification of Bit-Vector Arithmetic using Finite Integer Algebras", delivered at the Intl. Workshop on Constraints in Formal Verification (CFV), Sydney, Australia, August 2008.
- Invited Seminar, "Solving Bit-Vector Arithmetic", Calypto Design Systems, Nov 2007.
- Invited Panelist, NSF-Advance Workshop on CAREER Proposal Writing, Utah State University, March 2007.
- Graduate Seminar Series, "Synthesis and Verification of Arithmetic Datapaths using Finite Ring Algebra", Dept. of Mathematics and Statistics, Georgia State University, April 2006.
- Graduate Seminar Series, "Synthesis and Verification of Arithmetic Datapaths using Finite Ring Algebra", Dept. of Electrical and Computer Engineering, University of Massachusetts, March 2006.

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- Available upon request.