Erik Brunvand

As of Jan, 2017

Education

Ph.D., Computer Science, Carnegie Mellon University, 1991
Dissertation title: Translating Concurrent Communicating Programs into Asynchronous Circuits
Advisor: Robert F. Sproull

M.S., Computer Science, University of Utah, 1984
Thesis title: Context Addressable Memory for Symbolic Processing Systems

B.S., Computer Science, University of Utah, 1982 (*Magna cum Laude*)
B.S., Mathematics, University of Utah, 1982 (*Magna cum Laude*)

Professional Employment

Current
June 1990 to Present, Associate Professor of Computer Science, University of Utah (Assistant Professor from 1990-1996)

July 1999 to Present, Adjunct Associate Professor of Electrical and Computer Engineering, University of Utah.

July 2015 to Present, Director, Computer Engineering Program, University of Utah.

Previous
2014-2016, University Professor, University of Utah

Fall 2012, visiting professor, University of Washington, Seattle, Washington (sabbatical leave).

July 2002 to Sept 2005, July 2009 to 2012, Director, Computer Engineering Program, College of Engineering, University of Utah.

Spring 2006, visiting professor, Columbia University, New York, New York (sabbatical leave).

Fall, 2005, visiting professor, Max Planck Institut fuer Informatik, University of Saarland, Saarbruecken, Germany (sabbatical leave).

Winter, Spring 1999, visiting professor, University of Manchester, Manchester, England (sabbatical leave).

Fall 1998, visiting professor, University of Washington, Seattle (sabbatical leave).

September 1984 to May 1990, Research Assistant, Carnegie Mellon University.

Summer 1986, 1987, Student Intern with Sutherland, Sproull and Associates (Pittsburgh, PA).

Summer 1984, Student Intern with Evans and Sutherland Co. (Salt Lake City, UT).

Scholarship

Publications — Books

1. Erik Brunvand, *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Addison-Wesley, 2010.*

Publications — Refereed Journals

1. D. Kopta, K. Shkurko, J. Spjut, E. Brunvand, A. Davis. "Memory Considerations for Low-Energy Ray Tracing," Computer Graphics Forum, Vol34, No. 1, Feb 2015
2. E. Brunvand, "Speculatorum Oculi," Leonardo, Vol 47, No. 4, Aug 2014
3. E. Brunvand, A, Denyer,"Micro-Scale Printmaking on Silicon," Leonardo, Vol 44, No. 5, Sept/Oct 2011
4. D. Nellans, K. Sudan, E. Brunvand, R. Balasubramonian, "Improving Server Performance on Multi-Cores via Selective Off-loading of OS Functionality, LNCS 2010
5. Josef Spjut, Andrew Kensler, Daniel Kopta, and Erik Brunvand, "TRaX:, A Multicore Hardware Architecture for Real-Time Ray Tracing," IEEE Transacations on CAD, Vol 28, n12, Dec 2009.
6. David Nellans, Rajeev Balasubramonian, and Erik Brunvand, "OS Execution on Multi-Cores: Is Out-Sourcing Worthwhile?" ACM Operating Systems Review, Vol 43, No. 2, April 2009.
7. P. Shirley, K. Sung, E. Brunvand, A. Davis, S. Parker, S. Boulos, "Fast ray tracing and the potential effects on graphics and gaming courses," Computers & Graphics 32 (2), 2008.
8. Ganesh Gopalakrishnan, Prabhakar Kudva, and Erik Brunvand, "Peephole Optimization of Asynchronous Macromodule Networks," IEEE Transactions on VLSI Systems, Vol. 7, No. 1, March 1999.
9. William Richardson and Erik Brunvand, "Fred: A Decoupled Self-Timed Computer Architecture with Precise Exceptions," IEE Proceedings on Computers and Digital Techniques, Special issue on Asynchronous Processors. Vol. 143, No. 5, September 1996.
10. V. Chandramouli, Erik Brunvand, and Kent Smith, "Self-Timed Design in GaAs - Case Study of a High-Speed Parallel Multiplier," *IEEE Transactions on VLSI Systems*, March 1996.
11. Ganesh Gopalakrishnan, Erik Brunvand, Nick Michell, and Steve Nowick, "A Correctness Criterion for Asynchronous Circuit Validation and Optimization", *IEEE Transactions on Computer Aided Design* V13, n11, November 1994.
12. Erik Brunvand, "Designing Self-Timed Systems using Concurrent Programs," *Journal of VLSI Signal Processing*, 7, 1994, Special issue on asynchronous systems.
13. Erik Brunvand, "Using FPGAs to Implement Self-Timed Systems," *Journal of VLSI Signal Processing*, 6, 1993, Special issue on FPGAs.

Publications — In Books

1. John Hurdle, Lüli Josephson, and Erik Brunvand, "Reliable Interfacing of Self-Timed FPGA-based Neural Classifiers to Synchronous Parts," In "More FPGAs" Abingdon EE&CS Books, Abington, England 1994, Will R. Moore and Wayne Luk, Editors.
2. Erik Brunvand, "Windchime: An FPGA-based Self-Timed Parallel Processor," In "More FPGAs" Abingdon EE&CS Books, Abington, England 1994, Will R. Moore and Wayne Luk, Editors.
3. Erik Brunvand, "Implementing Self-Timed Systems with FPGAs", In "FPGAs" Abingdon EE&CS Books, Abington, England 1991, Will R. Moore and Wayne Luk, Editors.

Guest Editor of Journals

1. Erik Brunvand, Steve Furber, and Takashi Nanya eds., Special issue on Asynchronous Computer Architecture, *IEE Journal on Computers and Digital Techniques*. Special issue on Asynchronous Processors. Vol. 143, No. 5, September 1996.
2. Erik Brunvand, Ganesh Gopalakrishnan eds., Special issue on asynchronous circuits and systems, *Integration: The VLSI Journal*. vol 15 (1993).

Publications — Refereed Conferences

1. E. Brunvand and N. McCurty, "Making Noise: Using Sound-Art to explore Technological Fluency," ACM SIGCSE, Seattle, WA, 2017. *Awarded Best Paper*
2. D. Kline, N. Parshook, X. Ge, E. Brunvand, R. Melhem, P. Chrysanthis and A. Jones, "Holistically Evaluating the Environmental Impacts in Modern Computing Systems," International Sustainable and Green Computing (ICSG) Conference, Hangzhou, China, Nov 2016.
3. J G Alford and Erik Brunvand, "Leveraging CS Teachable Moments in the Maker Movement," ACM SIGCSE, Memphis, TN, 2016.
4. Erik Brunvand, "CS+X: Cross Campus Collaborations," ACM SIGGRAPH 2016 (panel), Anaheim, CA, August 2016.
5. E. Brunvand, "Kinetic Sculptures: Creating Programmable Art," ACM SIGGRAPH 2015 (course), Los Angles, CA, August 2015.
6. E. Brunvand, "A Noise-Based Curriculum for Technological Fluency," ACM SIGGRAPH 2015 (talk), Los Angeles, CA, August 2015.
7. E. Brunvand, "Using Surface-Mount Components in an Embedded Systems Lab," ACM Workshop on Computer Architecture Education (WCAE), Portland, OR, June 2015.
8. E. Brunvand, "Technological Fluency through Circuit Bending," International Conference on Microelectronic Systems Education, Pittsburgh, PA, May 2015.

9. E. Brunvand, N. Chatterjee, D. Kopta, “Why Graphics Programmers Need to Know about DRAM,” SIGGRAPH 2014 (course), Vancouver, B.C., Canada.

10. E. Brunvand and S. Brunvand, “Drawing Machines: An Arts and Engineering Collaboration,” NAEA conference, San Diego, CA, Mar 2014

11. E. Brunvand, “Automated Drawing: Exploring the Boundaries between Print and Drawing,” Impact8, Dundee, Scotland, August 2013.

12. E. Brunvand, “Electrified Printmaking: Using Conductive Ink to Create Active Images,” Impact8, Dundee, Scotland, August 2013.

13. Daniel Kopta, Konstantin Shkurko, Josef Spjut, Erik Brunvand, Al Davis, “An Energy and Bandwidth Efficient Ray Tracing Architecture,” in High-Performance Computer Graphics (HPG 2013), July 2013.

14. Erik Brunvand, “Lights! Speed! Action!: Fundamentals of physical computing for programmers,” in *ACM SIGGRAPH 2013 Courses*, SIGGRAPH ’13, (New York, NY, USA), pp. 13:1–13:108, ACM, 2013.

15. Erik Brunvand, “Arts/tech collaboration with embedded systems and kinetic art,” in *ACM SIGGRAPH 2013 Talks*, SIGGRAPH ’13, (New York, NY, USA), pp. 23:1–23:1, ACM, 2013.

16. E. Brunvand, J. G. Alford, and P. Stout, ”Drawing machines: Exploring embedded system programming and hardware with an artistic flair,” SIGCSE, Denver, CO, 2013

17. Erik Brunvand, “Automated Drawing Machines: Blurring the Line between Drawing and Print,” Southern Graphics Council International (SGCI) conference, Mar 2013.

18. Konstantin Shkurko, Thiago Ize, Christiaan Gribble, Erik Brunvand, and Lee Butler, “Simulating Radio Frequency Propagation via Ray Tracing,” GPU Technology Conference, March 2013 (poster).

19. Erik Brunvand, Paul Stout, Jennifer Alford, “Drawing Machines: Exploring embedded system programming and hardware with an artistic flair,” ACM SIGCSE Symposium on Computer Science Education (3-hour workshop, referred acceptance), Mar 2013.

20. Daniel Kopta, Thiago Ize, Josef Spjut, Erik Brunvand, Al Davis, Andrew Kensler, “Fast, Effective BVH Updates for Animated Scenes,” ACM SIGGRAPH Symposium on Interactive 3D Graphics and Games (I3D), Mar, 2012.

21. Joseph Spjut, Daniel Kopta, Erik Brunvand, Al Davis, “A Mobile Accelerator Architecture for Ray Tracing,” 3rd Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW-3), Feb 2012.

22. Erik Brunvand, Paul Stout, “Collaborative Design Experience with Kinetic Sculpture.” College Art Association (CAA), Feb 2012.

23. Erik Brunvand, Al Denyer, “Printmaking on a Micro Scale: An Art and Science Collaboration ,” Southeastern College Art Conference (SECAC), Nov 2011.

24. E. Brunvand, “Games as Motivation in Computer Design Courses: I/O is the Key,” SIGCSE, Dallas, March 2011.

25. E. Brunvand, P. Stout, “Kinetic Art and Embedded Systems: A Natural Collaboration,” SIGCSE, Dallas, March 2011.

26. D. Kopta, J. Spjut, E. Brunvand, A. Davis, “Efficient MIMD Architectures for High-Performance Ray Tracing,” International Conference on Computer Design (ICCD), Oct 2010.

27. D Nellans, K. Sudan, E. Brunvand, R. Balasubramonian, "Improving Server Performance on Multi-Cores via Selective Off-loading of OS Functionality, WIOSCA, June 2010.

28. D Nellans, K. Sudan, E. Brunvand, R. Balasubramonian, "Hardware Prediction of OS Run-Length for Fine-Grained Resource Customization,: ISPASS, March 2010.

29. E. Brunvand, A. Denyer "Printmaking at a Micro Scale," Impact Conference, Bristol, U.K., September 2009.

30. D. Kopta, J. Spjut, and E. Brunvand, "Grid-based Ray Tracing with CUDA," ACM/Eurographics High Performance Graphics, New Orleans, August 2009.

31. J. Spjut, A. Kensler, and E. Brunvand, "Hardware-Accelerated Gradient Noise for Graphics," ACM Great Lakes Conference on VLSI (GLSVLSI09), May 2009.

32. E Brunvand, "Printmaking with Extreme Technology, Southern Graphics Council Conference, Chicago, March 2009.

33. D. Kopta, J. Spjut, E. Brunvand, and S. Parker, "Comparing Incoherent Ray Performance of TRaX vs. Manta," *IEEE Symposium on Interactive Ray Tracing*, August 2008.

34. J. Spjut, D. Kopta, S. Boulos, S. Kellis, and E. Brunvand, "TRaX: A multi-threaded architecture for real-time ray tracing," In *6th IEEE Symposium on Application Specific Processors (SASP)*, June 2008 *Winner of Best Paper award for SASP08*.

35. P. Shirley, K. Sung, E. Brunvand, A. Davis, S. Parker, S. Boulos, "Rethinking Graphics and Gaming Courses Because of Fast Ray Tracing", *SIGGRAPH Educator's Workshop*, 2007.

36. Sven Woop, Erik Brunvand, and Philipp Slusallak, "Estimating Performance of an Ray Tracing ASIC Design," IEEE Symposium on Interactive Ray Tracing (RT06), September 2006.

37. Jung-Lin Yang and Erik Brunvand, "Improved Technique on Parallelism for Asynchronous Controllers," 17th VLSI Design / CAD Symposium, 2006.

38. Jung-Lin Yang, Erik Brunvand, and Sung-Min Lin, "HDL Modeling for Optimization and Verification of Asynchronous Controllers," International Symposium on Intelligent Signal Processing and Communication Systems, ISPACS 2005, Hong Kong, December 2005.

39. Jung-Lin Yang and Erik Brunvand, "Self-Timed Circuits Using DCVSL Semi-Bundled Delay Wrappers," International Symposium on Intelligent Signal Processing and Communication Systems, ISPACS 2005, Hong Kong, December 2005.

40. David Nellans, Rajeev Balasubramonian and Erik Brunvand, "A Case for Increased Operating System Support in Chip Multi-Processors," Second IBM Watson Conference on Interaction between Architecture, Cicuits, and Compilers, PAC^2, New York, September 2005.

41. Gaurav Gulati and Erik Brunvand, "Design of a Cell Library for Asynchronous Microengines," Great Lakes Symposium on VLSI, April 2005.

42. Jung-Lin Yang and Erik Brunvand, "Pseudo Dynamic DCVSL Template For Power-Conservative Design," 16th VLSI Design / CAD Conference, 2005

43. Jung-Lin Yang, Erik Brunvand, and Sung-Min Lin, "HDL Modeling for Optimization and Verification Of Extended Burst-Mode Machines," 16th VLSI Design / CAD Conference, 2005

44. Niti Madan and Erik Brunvand, "Asynchronous Microengines for Network Processing," International Conference on Information Systems: New Generations (ISNG 2004), Las Vegas, November 2004.

45. Niti Madan and Erik Brunvand, "A Case for Asynchronous Microengines for Network Processors," Advanced Networking and Communications Hardware Workshop (ANCHOR) 2004, Munich, Germany, June 2004

46. David Nellans, Vamshi Kadaru, and Erik Brunvand, "ARCsim: An Asynchronous Architectural Simulator," Great Lakes Symposium on VLSI, April 2004.

47. Jung-Lin Yang and Erik Brunvand, "Using Dynamic Domino Circuits in Self-Timed Systems," Great Lakes Symposium on VLSI, April 2003.

48. Jung-Lin Yang and Erik Brunvand, "Self-Timed Design with Dynamic Domino Circuits," IEEE Annual Symposium on VLSI Design, February 2003.

49. Hans Jacobsen, Erik Brunvand, Ganesh Gopalakrishnan, and Prabhakar Kudva, "High Level Asynchronous System Design Using the ACK Framework," In International Conference on Advanced Research in Asynchronous Circuits and Systems (Async2000), Eilat, Israel, April 2000.

50. Erik Brunvand, Steven Nowick, and Kenneth Yun, "Tutorial on Practical Asynchronous Circuit Design," Design Automation Conference, DAC-99, New Orleans, LA, June 1999.

51. Erik Brunvand, Steven Nowick, and Kenneth Yun, "Modern Asynchronous Circuit Design," TAU-99, Monteray, CA, March 1999.

52. J. Carter, W. Hsieh, L. Stoller, M. Swanson, L. Zhang, E. Brunvand, A. Davis, C.-C. Kuo, R. Kuramkote, M. Parker, L. Schaelicke, and T. Tateyama, "Impulse: Building a Smarter Memory Controller," The Proceedings of the Fifth Internationl Symposium on High Performance Computer Architecture, Jan 1999

53. J. Carter, W. Hsieh, M. Swanson, L. Zhang, E. Brunvand, A. Davis, M. Parker, L. Schaelicke, L. Stoller, and T. Tateyama. "Memory System Support for Irregular Applications," Fourth Workshop on Languages, Compilers, and Run-time Systems for Scalable Computers (LCR '98), May 1998.

54. Erik Brunvand, Steven Nowick, and Kenneth Yun, "Practical Advances in Asynchronous Circuits and Systems," International Conference on Computer Design (ICCD 97), pp 662–668.

55. Erik Brunvand, "Bugs and Glitches in Computer Folklore", American Folklore Society, Austin TX, October 1997.

56. Ajay Khoche and Erik Brunvand, "Critical Hazard-Free Test Generation for Asynchronous Circuits," VLSI Test Symposium (VTS'97), pp 203–208.

57. Ajay Khoche and Erik Brunvand, "ACT: A DFT Tool for Self-Timed Circuits," International Test Conference (ITC'97), pp 829–837.

58. Erik Brunvand, "The Heroic Hacker: Legends of the Computer Age," American Folklore Society, Pittsburgh PA, October 1996.

59. William Richardson and Erik Brunvand, "Fred: A Decoupled Self-Timed Computer," In International Conference on Advanced Research in Asynchronous Circuits and Systems (Async96), Aizu, Japan, March 1996.

60. Sandeep Pagey, Ajay Khoche and Erik Brunvand, "DFT for Fast Testing of Self-Timed Control Circuits," 4th IEEE Asian Test Symposium, 1995.

61. William Richardson and Erik Brunvand, "Precise Exception Handling for a Self-Timed Processor," in IEEE International Conference on Computer Design (ICCD95) *Winner of best paper award in Design & Test track at ICCD95*.

62. Ajay Khoche and Erik Brunvand, "Testing Self-Timed Circuits using Partial Scan," in 2nd Working Conference on Asynchronous Design Methodologies, South Bank University, London, May 1995.

63. Ajay Khoche and Erik Brunvand, "A Partial-Scan Methodology for Testing Self-Timed Circuits," in 13th IEEE VLSI Test Symposium, Princeton, NJ, April 1995.

64. Erik Brunvand, "Low Latency Self-Timed Flow Through FIFOs," in 16th Conference on Advanced Research in VLSI, Chapel Hill, NC, March 1995.

65. Jae-Tack Yoo, Erik Brunvand, and Kent Smith, "Automatic Prototyping of Semi-Custom Integrated Circuits using Actel FPGAs," in Fifth Great Lakes Symposium on VLSI, Buffalo, NY, March 1995.

66. Ajay Khoche and Erik Brunvand, "Testing Micropipelines," In International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async94), November 1994.

67. Ganesh Gopalakrishnan, Prabhakar Kudva, and Erik Brunvand, "Peephole Optimization of Asynchronous Macromodule Networks," In IEEE International Conference on Computer Design (ICCD), 1994.

68. Prabhakar Kudva, Ganesh Gopalakrishnan, and Erik Brunvand, "Performance Analysis and Optimization of Asynchronous Circuits," In IEEE International Conference on Computer Design (ICCD), 1994. pages)

69. Joe Novak and Erik Brunvand, "Using FPGAs to Prototype a Self-Timed Floating Point Co-Processor," In IEEE Custom Integrated Circuits Conference (CICC), 1994.

70. Lüli Josephson, Erik Brunvand, John F. Hurdle, and Ganesh Gopalakrishnan, "Reliable Interface Design for Combining Asynchronous and Synchronous Circuits," In Fifth NASA Symposium on VLSI Design, Albuquerque, New Mexico. November 1993.

71. John F. Hurdle, Peter Conwell, and Erik Brunvand, "Robust Neural Classifier Circuits using Asynchronous Design," In Fifth NASA Symposium on VLSI Design, Albuquerque, New Mexico. November 1993.

72. Ajay Khoche and Erik Brunvand, "Testing Self-Timed Circuits using Scan Paths," In Fifth NASA Symposium on VLSI Design, Albuquerque, New Mexico. November 1993.

73. Erik Brunvand, "Windchime: An FPGA-based Self-Timed Parallel Processor," In 3rd International Workshop on Field Programmable Logic and Applications, Oxford, September, 1993.

74. John F. Hurdle, Lüli Josephson and Erik Brunvand, "Reliable Interfacing of Self-Timed FPGA-based Hybrid Neural/Rule-Based Classifiers to Synchronous Co-Processors," In 3rd International Workshop on Field Programmable Logic and Applications, Oxford, September, 1993.

75. Erik Brunvand, "The NSR Processor," In 26th Hawaiian International Conference on System Sciences, Maui, Hawaii, Jan 1993.

76. John F. Hurdle, Erik Brunvand, Lüli Josephson, and Ganesh Gopalakrishnan, "Asynchronous Models for Large Scale Neurocomputing Applications," In Fifth International Conference on Neural Networks and their Applications, Nimes, France, November 1992.

77. Erik Brunvand, Nick Michell, and Kent Smith, "A Comparison of Self-Timed Design using FPGA, CMOS, and GaAs Technologies," In IEEE International Conference on Computer Design (ICCD), Cambridge, Mass., October 1992.

78. John F. Hurdle, Erik Brunvand, and Lüli Josephson, "Asynchronous VLSI Design for Neural System Implementation," In Third International Workshop on VLSI for Neural Networks and Artificial Intelligence, Oxford, September 1992.

79. Erik Brunvand, "Using FPGAs to Prototype a Self-Timed Computer," In 2nd International Workshop on Field-Programmable Logic and Applications, Vienna Institute of Technology, August 1992.

80. Erik Brunvand, "Implementing Self-Timed Systems with FPGAs," In International Workshop on Field Programmable Logic and Applications, Oxford, September, 1991.

81. Erik Brunvand and Mike Starkey, "An Integrated Environment for the Design and Simulation of Self-Timed Systems," In *VLSI-91*, IFIP, August 1991.

82. Erik Brunvand and Robert F. Sproull, "Translating Concurrent Programs into Delay-Insensitive Circuits," In IEEE International Conference on Computer-Aided Design *ICCAD-89*, November 1989.

Publications — Technical Reports

1. Daniel Kopta, Andrew Kensler, Thiago Ize,Josef Spjut, Erik Brunvand, Al Davis, "Fast, Effective BVH Updates for Dynamic Ray-Traced Scenes Using Tree Rotations," University of Utah, School of Computing, UUCS-11-002, 2011.

2. David Nellans, Rajeev Balasubramonian, and Erik Brunvand, "Interference Aware Cache Designs for Operating System Execution," University of Utah, School of Computing, UUCS-09-002, 2009.

3. Sven Woop, Erik Brunvand, and Philipp Slusallek, "HWML: RTL/Structural Hardware Description using ML," Technical Rrport, Computer Graphics Lab, Saarland University, 2006.

4. Gaurav Gulati and Erik Brunvand, "A Cell Library for Asynchronous Microengines," Technical Report, University of Utah, School of Computing, Jan 2005.

5. Franklin Prosser, David Winkel, and Erik Brunvand, "A comparison of modular self-timed design styles," University of Utah, Department of Computer Science, UUCS-95-025.

6. William F. Richardson and Erik Brunvand, "Fred: An Architecture for a Self-Timed Decoupled Computer," Technical Report UUCS-95-008, University of Utah, Department of Computer Science, 1995.

7. Ajay Khoche and Erik Brunvand, "A Partial Scan Methodology for Testing Self-Timed Circuits," Technical Report UUCS-95-001, University of Utah, Department of Computer Science, 1995.

8. Erik Brunvand, "Reduced Latency Self-Timed FIFO Circuits," Technical Report UUCS-94-037, University of Utah, Department of Computer Science, 1994.

9. Jae-Tack Yoo, Erik Brunvand, and Kent Smith, "Automatic Rapid Prototyping of Semi-Custom VLSI Circuits using FPGA's," Technical report UUCS-94-022, University of Utah, Department of Computer Science, 1994.

10. Prabhakar Kudva, Ganesh Gopalakrishnan, and Erik Brunvand, "Performance Analysis and Optimization of Asynchronous Circuits," Technical Report UUCS-94-015, University of Utah, 1994.

11. Nick Michell, Erik Brunvand, and Kent Smith, "A Gallium Arsenide Mutual Exclusion Element," Technical Report UUCS-93-029, University of Utah, Department of Computer Science, 1993.

12. Erik Brunvand and Nick Michell, "Speed without Fear: Composable Self-Timed GaAs Circuits," Technical Report UUCS-93-028, University of Utah, Department of Computer Science, 1993.

13. Ganesh Gopalakrishnan, Erik Brunvand, and Nick Michell, “A Correctness Criterion for Asynchronous Circuit Validation and Optimization,” Technical Report UUCS-92-004, University of Utah, 1992.

14. William Richardson and Erik Brunvand, “The NSR Processor Prototype,” Technical Report UUCS-92-029, University of Utah, Department of Computer Science, 1992.

15. Erik Brunvand, “A Cell Set for Self-Timed Design using Actel FPGAs,” Technical Report UUCS-91-013, University of Utah, Department of Computer Science, 1991.

16. Erik Brunvand and Robert F. Sproull, “Translating Concurrent Communicating Programs into Delay Insensitive Circuits,” Technical Report CMU-CS-89-126, Carnegie Mellon University, 1989.

17. Erik Brunvand, “Parts-R-Us: A Chip Aparts,” Technical Report CMU-CS-87-119, Carnegie Mellon University, 1987.

18. Erik Brunvand and Ivan E. Sutherland, “An Asynchronous Q-Bus Interface,” Technical Memo 4677, Sutherland, Sproull, and Associates, 1986.

Publications — Other

1. Erik Brunvand, “Translating Concurrent Communicating Programs into Asynchronous Circuits,” Ph.D. Dissertation, Carnegie Mellon University, 1991 (Available as Technical Report CMU-CS-91-198). pages)

2. Erik Brunvand, “Context Addressable Memory for Symbolic Processing Systems,” Masters Thesis, University of Utah, 1984.

Patents

1. Erik Brunvand and Alan Davis, “Circulating Context Addressable Memory,” U.S. Patent No. 4,924,435, issued May 8 1990.

2. Erik Brunvand, Alan Davis, and Ian Robinson, “Memory Apparatus and Method for Retrieving Sequences of Symbols Including Variable Elements,” U.S. Patent No. 4,748,439, issued May 31, 1988.

Keynote Addresses

1. “Computational Thinking Meets Design Thinking: Technology and Arts Collaborations,” VLSI Design / CAD Conference, Kolkata, India, January 2016.

2. “Computational Thinking Meets Design Thinking: Technology and Arts Collaborations,” ACM Great Lakes Symposium on VLSI, Pittsburgh, PA, May 2015.

3. “Twenty Years of Async,” IEEE Symposium on Asynchronous Circuits and Systems, Potsdam, Germany ,May 2014.

4. “The Heroic Hacker: Computer Folklore and Hacker Culture,” IEEE Symposium on Asynchronous Circuits and Systems, Santa Monica, CA, May 2013.
5. “High Performance Ray Tracing: Implications for System Architectures,” IEEE/IFIP VLSI-SoC conference, Oct 2012.

Invited Talks

“A Tale of Two Rendering Algorithms: Ray Tracing, Rasterization, and their Supporting Hardware,” University of Richmond, Richmond, VA, January 2017.

“Drawing Machines: An Arts and Engineering Collaboration,” Visiting artist lecture, Frostic School of the Arts, Western Michigan University, Kalamazoo, MI, April 2015.

“ Drawing Machines: Mechanical Computer Graphics,” Studio workshop and contest, SIGGRAPH, Vancouver, Canada, 2014

“Drawing Machines and Arts Tech Collaborations,” Snow College visiting artists lecture series, Ephraim, UT, April, 2014

“Design Thinking meets Computational Thinking: Kinetic Art and Embedded Systems,” Newcastle University, Newcastle, U.K., August 2013

“Arts and Technology: Strange Bedfellows or Congenial Colleagues?,” Western State Colorado University, Gunnison, Colorado, April, 2013

“Embedded Systems and Kinetic Art,” University of Washington, Seattle, Nov 2012.

“Arts and Technology: Strange Bedfellows or Congenial Colleagues?,” College of Charleston, Nov 2011.

“Hardware Support for Interactive Ray Tracing,” Columbia University, New York, February 2006.

“Asynchronous and Self-Timed System Design,” University of Saarland, October 2005.

“A New Course in Arithmetic Circuits,” David Evans Conference on Computer Engineering, Midway, Utah, June 2005

“A Computer Engineering Grad Curriculum” David Evans Conference on Computer Engineering, Midway, Utah, June 2004.

“Teaching VLSI: CAD Tools, Chips and Challenges,” David Evans Conference on Computer Engineering, Midway, Utah June 2003.

“Fred, an Asynchronous Microprocessor,” Computer Science Department, South Bank University, London, England, May 1999.

“Asynchronous Processor Design,” Computer Science Department, South Bank University, London, England, April 1999.

“Fred, an Asynchronous Microprocessor,” Computer Science Department, University of Manchester, Manchester, England, April 1999.

"Asynchronous Processor Design," Computer Science Department, University of Manchester, Manchester, England, March 1999.

"Modern Asynchronous Circuit Design," Computer Science Department, University of Washington, Seattle, November 1998.

"The Avalanche Multiprocessor," Computer Science Department, Carnegie Mellon University, October 1996.

"Self-Timed Circuits and FIFOs," Electrical Engineering Department, Cornell University, October 1995.

"The State of Self-Timed Circuit Design," Keynote speaker for the 2nd Working Conference on Asynchronous Design Methodologies, South Bank University, London, May 1995.

"Self-Timed Circuits and FPGAs," Computer Science Department, University of Waterloo, Waterloo, Canada, April 1994.

"Windchime: A Self-Timed Parallel Computer," Computer Science Department, Technical University of Denmark, Lyngby, Denmark, September 1993.

"The NSR Processor Architecture," Computer Science Department, University of Manchester, Manchester, England, August 1993.

"The NSR Processor Architecture," Sun Microsystems Laboratories, Mountain View, CA, November 1992.

"The NSR Processor FPGA Prototype," Actel Corporation, Sunnyvale, CA, November 1992.

"Implementing Self-Timed Circuits with FPGAs," DEC Paris Research Labs, Paris, France, August 1992.

"The NSR Processor," Computer Science Department, Stanford University, Stanford, CA, July 1992.

"The NSR Processor FPGA Prototype," National Science Foundation, workshop on Integrating FPGAs Into Microelectronics Education, Washington, D.C., July 1992.

"Translating Concurrent Programs into Asynchronous Circuits," Computer Science Department, University of Washington, Seattle, WA, September 1989.

"Translating OCCAM programs into Self-Timed Circuits," HP Labs, Palo Alto, CA, August 1989.

"Translating OCCAM programs into Self-Timed Circuits," Apple Computer, Advanced Technology Group, Cupertino, CA, August 1989.

Research

Current Research Support

Title:	Architectures for Energy Efficient Ray Tracing
Agency:	National Science Foundation
Total Award:	$899,992
Duration:	October 2014 — September 2018
Principal Investigator:	Erik Brunvand
Co-PIs:	Cem Yuksel, Al Davis

Past Research Support

Title:	Radio Frequency Ray Tracing
Agency:	Army Research Labs (ARL)
Total Award:	$85,000
Duration:	September 2012 — September 2013 (recurring award)
Principal Investigator:	Erik Brunvand

Title:	Flexible Architectures for Future Graphics Processing Systems
Agency:	National Science Foundation
Total Award:	$499,709
Duration:	August 2010 — July 2014
Principal Investigator:	Erik Brunvand, Co-Pi Al Davis

Title:	Radio Frequency Ray Tracing Evaluation
Agency:	Army Research Labs
Total Award:	$37,384
Duration:	February 2011 — May 2011
Principal Investigator:	Erik Brunvand

Title:	Hardware Support for Real Time Ray Tracing
Agency:	National Science Foundation
Total Award:	$505,382
Duration:	June 2006 — June 2010
Principal Investigator:	Erik Brunvand, Co-Pis Al Davis, Pete Shirley, Steve Parker

Title:	Ray Trace Applications to Radio Frequency (RF) Propogation
Agency:	Army Research Labs (ARL)
Total Award:	$140,087
Duration:	September 2007 — December 2008
Principal Investigator:	Erik Brunvand

Title:	High-Performance Asynchronous Computer Architecture
Agency:	National Science Foundation
Total Award:	$325,000
Duration:	September 2002 — July 2006
Principal Investigator:	Erik Brunvand

Title:	Microengines for Programmable Self-Timed Control
Agency:	National Science Foundation
Total Award:	$412,914
Duration:	September 2000 — July 2004
Principal Investigator:	Erik Brunvand
Co-PI:	Ganesh Gopalakrishnan

Title:	Impulse: Adaptive Memory Systems
Agency:	ARPA, Adaptive Computer Systems
Total Request:	$2,700,000
Duration:	Started January 1998, 3 years
Principal Investigator:	John Carter
Original Co-PIs:	Erik Brunvand, Mark Swanson

Title:	Center of Excellence in Asynchronous Circuit and System Design
Agency:	Utah State Centers of Excellence Program
Current Award:	$100,000 per year, renewable annually
Total Award:	$300,000, Renewed for three years, 1997-2000.
Duration:	Started July 1997, renewed for three years
Principal Investigators:	Erik Brunvand, Chris Myers (EE)

Title:	Application-Driven Advancement of Asynchronous Design Methods
Agency & Award Number:	National Science Foundation MIP-9622587
Total Award:	$503,291
Duration:	Sept 1996 — July 2000
Principal Investigator:	Erik Brunvand
Co-PI:	Ganesh Gopalakrishnan

Title:	Communication and Memory Architectures for Scalable Parallel Computing (Avalanche)
Agency & Award Number:	ARPA/SPAWAR, Contract N0039-95-C-0018
Total Award:	$4,700,000
Duration:	Sep 1995 — Dec 1998
Principal Investigator:	Al Davis
Co-PIs:	Erik Brunvand, John Carter, Mark Swanson

Title:	Advanced Research in Asynchronous Circuits and Systems
Agency & Award Number:	National Science Foundation MIP-9406532
Total Award:	$12,320 to help support an international conference on asynchronous circuit design held in Salt Lake City in November 1994
Duration:	Nov 1994 — Jul 1995
Principal Investigator:	Erik Brunvand
Co-PIs:	Ganesh Gopalakrishnan, Steve Nowick (Columbia University)

Title:	The Design of Asynchronous Circuits and Systems with Emphasis on Correctness and Proven Optimizations
Agency & Award Number:	National Science Foundation MIP-9215878
Total Award:	$240,000
Duration:	Jan 1993 — Jun 1996
Principal Investigator:	Erik Brunvand
Co-PI:	Ganesh Gopalakrishnan

Title:	Testing Asynchronous Circuits
Agency:	University of Utah Research Committee
Total Award:	$5,000
Duration:	Sep 1993 — Sep 1995
Principal Investigator:	Erik Brunvand

Title:	Self-Timed GaAs Building Blocks for High performance Systems
Agency & Award Number:	National Science Foundation grant MIP-9115372
Total Award:	$110,000
Duration:	Jan 1992 — Jun 1994
Principal Investigator:	Kent Smith
Co-PI:	Erik Brunvand

Title:	Asynchronous Computer Architecture
Agency & Award Number:	National Science Foundation Research Initiation Award MIP-9111793
Total Award:	$70,000 + $10,000 university matching funds for equipment
Duration:	Aug 1991 — Jan 1994
Principal Investigator:	Erik Brunvand

Title:	Building Blocks for Implementing Self Timed VLSI Circuits
Agency:	Utah Research Committee
Total Award:	$5,000
Duration:	Feb 1991 — Feb 1993
Principal Investigator:	Erik Brunvand

Title:	Using FPGAs in the Classroom
Agency:	National Science Foundation
Total Award:	$6,000 equipment gift
Duration:	Sep 1990
Principal Investigator:	Erik Brunvand

Other Research Support (Gifts, Conference Support, etc)

Title:	Conference support for IEEE Symposium on Asynchronous Circuits and Systems
Agency:	Oracle
Total Award:	$ 24,000 total, $6,000 in 2015, 2016, $3,000 in each of four previous years (2014, 2013, 2012, 2011)
Principal Investigator:	Erik Brunvand

Title:	Cadence Design Flow Support
Agency:	Cadence Inc.
Total Award:	$2,000
Duration:	Unrestricted gift, received December 2005
Principal Investigator:	Erik Brunvand

Title:	Student Participation Support for the ASYNC 2001 Symposium at the University of Utah.
Agency:	Sun Microsystems
Total Award:	$20,000
Duration:	Conference was in March 2001
Principal Investigator:	Erik Brunvand

Title:	Support for ASYNC 2001 Symposium at the University of Utah
Agency:	Intel Corporation
Total Award:	$2,000
Duration:	Conference was in March 2001
Principal Investigator:	Erik Brunvand

Title:	Support for ARVLSI 2001 Conference at the University of Utah
Agency:	Intel Corporation
Total Award:	$1,500
Duration:	Conference was in March 2001
Principal Investigator:	Erik Brunvand

Chairman of Doctoral Thesis Committee

Current Students

Konstantin Shkurko (Ph.D., Expected 2017)

Tim Grant (Ph.D. Expected 2019)

Graduated Students

Daniel Kopta (Ph.D., 2015), "Ray Tracing from a Data Movement Perspective."

David Nellans (Ph.D., 2014), "Improving Operating System and Hardware Interaction."

Josef Spjut (Ph.D., 2013), "Hardware Support for Real Time Ray Tracing."

Jung-Lin Yang (Ph.D., 2003), "Transistor Level Technology Mapping for Extended Burst-Mode Asynchronous Designs," (Electrical and Computer Engineering Department).

Lüli Josephson (M.Phil.,2001)

Ajay Khoche (Ph.D., 1996) "Testing Asynchronous Circuits,"

Bill Richardson (Ph.D., 1996) "Architectural Considerations in a Self-Timed Processor Design,"

John Hurdle (Ph.D., 1994) "Smart Parts: Toward the Automated Synthesis of Neural Circuits,"

Chairman of Masters Thesis Committee

Graduated Students

Eli Ribble (M.S. 2009), "Visualizing 802.11 Wireless Connection Strength," School of Computing, University of Utah.

Ryan Romney (M.S. 2008), "Circuits for Computing Inverse Square Root." Electrical and Computer Engineering Department, University of Utah.

Gaurav Gulati (M.S. 2006) "A Cell Set and Library for Asynchronous Microengine Design," Electrical and Computer Engineering Department, Univerity of Utah.

Niti Madan (M.S. 2004) "Asynchronous Microengines for Network Processing"

Himanshu Singh (M.S. 2004) “Asynchronous Microengines for DSP Applications” (Electrical and Computer Engineering Department).

Sudeesh Madayi (M.E. 2003) (Electrical and Computer Engineering Department).

Vamshi Krishna Kadaru (M.E. 2003) (Electrical and Computer Engineering Department).

Mike Snider (M.E. 2003) (Electrical and Computer Engineering Department).

Harishankar Sridharan (M.E. 2002) (Electrical Engineering Department).

David LeBaron (M.E., 1997) (Electrical Engineering Department).

Joe Novak (M.S. 1994) “A Self-Timed IEEE Floating Point Unit,”

Tom Wolf (M.S. 1992) “The A3000: A Self-Timed Version of the R3000,”

Member of Doctoral Thesis Committee

(Needs updating...) Peter Jensen (Ph.D. Expected 2006), Hans Jacobson (Ph.D. 2003), Eric Mercer (Ph.D. 2002), Eric Peskin (Ph.D. 2002), Hao Zheng (Ph.D. 2001), Lambert Schaelicke (Ph.D. 2001), Ravi Kuramkote (Ph.D. 2001), Wendy Belluomini (Ph.D. 1999), Ravi Hosabetta (Ph.D. 1999), Nick Michell (Ph.D. 1997), Greg Hannon (M.Phil. 1996), Kelly Jones, (Ph.D. 1995), Prabhakar Kudva (Ph.D. 1995),

Member of Masters Thesis Committee

(Needs updating...) Anand Gopalan (M.S. 2002), Chris Krieger (M.S. 2001), Eric Mercer (M.S. 1999), Brandon Bachman (M.S. 1998), Robert Thacker (M.S. 1998), Hao Zhang (M.S. 1998), Richard G. Burford (M.S. 1995), “Asynchronous Logic Building Blocks for Pipelined DSP Applications,” External examiner for this thesis from The Flinders University of South Australia. Neil Bergman, Chair., Anthony Dobaj (M.S. 1995), Kyle Johns (M.S. 1994), V. Chandramouli (M.S. 1993), Madhu Penugonda (M.S. 1993), Prabhat Jain (M.S. 1992), Prabhakar Kudva (M.S. 1992),

Teaching

Detailed Teaching Data

Awarded two-year University Professorship from the Undergraduate College for the academic years 2014-2015 and 2015-2016.

Awarded School of Computing Outstanding Teaching Award, 2012.

Awarded University of Utah Distinguished Teaching Award for 2002-2003 (also nominated in 2001-2002).

IEEE Nominee for Utah Engineers Council, Engineering Educator of the Year award, 2003.

Awarded College of Engineering Outstanding Teaching Award for 1997.

Awarded 30 Dean's Teaching Commendation Letters for outstanding student course evaluations since 1990. These letters go to professors in the top 15% of the college based on teaching evaluation scores.

Date	Course Number	Course Name	Class Size	Comments
Spring 17	CS/ECE 3700	Digital System Design	92	
	CS 5789 / Art 4455	Embedded Systems & Kinetic Art	22	
Fall 16	CS/ECE 3991	Computer Engineering Jr. Seminar	27	
	CS/ECE 4710	Computer Engineering Sr. Project	23	Awarded Dean's Teaching Commendation
Spring 16	CS/ECE 3992	Computer Engineering Pre-Project	19	
	UGS/CS 2050	Making Noise: Sound Art and Digital Media	27	Awarded Dean's Teaching Commendation
Fall 15	CS/ECE 5710	Digital VLSI	16	Awarded Dean's Teaching Commendation
	CS/ECE 6710	Digital VLSI	60	Awarded Dean's Teaching Commendation
	CS/ECE 3991	Computer Engineering Jr. Seminar	23	
Spring 15	CS 5789	Embedded Systems and Kinetic Art	8	
	UGS 2050	Making Noise: Sound Art and Digital Media	20	
Fall 14	CS/ECE 4710	Computer Engineering Sr. Project	18	Awarded Dean's Teaching Commendation
Spring 14	CS/ECE 3992	Computer Engineering Pre-Project	23	
	CS 5789 / Art 4455	Embedded Systems & Kinetic Art	23	
	CS/ECE 6712	Digital IC Testing	8	
Fall 13	CS/EE 5710	Digital VLSI	17	Awarded Dean's Teaching Commendation
	CS/ECE 6710	Digital VLSI	35	
Spring 13	Sabbatical Leave			
Fall 12	Sabbatical Leave at University of Washington			

Date	Course Number	Course Name	Class Size	Comments
Spring 12	CS/EE 3700	Digital System Design	74	Awarded Dean's Teaching Commendation
	CS 5789 / Art 3490	Embedded Systems & Kinetic Art	23	
	CS/EE 6712	Digital IC Testing	6	
Fall 11	CS/EE 5710	Digital VLSI	13	Awarded Dean's Teaching Commendation
	CS/EE 6710	Digital VLSI	31	Awarded Dean's Teaching Commendation
	CS 6965	Parallel HW Ray Tracing	8	
	CS/ECE 3991	Computer Engineering Jr. Seminar	17	
Spring 11	CS/ECE 5830	VLSI Architecture	5	
	CS/ECE 6830	VLSI Architecture	21	
Fall 10	CS/ECE 3710	Computer Design Lab	20	Awarded Dean's Teaching Commendation
	CS5968/ART4455	Embedded Systems & Kinetic Art	20	
	CS/ECE 3991	Computer Engineering Jr. Seminar	21	
Spring 10	CS/EE 3700	Digital System Design	60	Awarded Dean's Teaching Commendation
	CS/EE 6712	Digital IC Testing	10	
Fall 09	CS/EE 5710	Digital VLSI	13	
	CS/EE 6710	Digital VLSI	31	Awarded Dean's Teaching Commendation
	CS/FA 5968/3800	Sp.Topics: Emb. Sys. & Kinetic Art	9	Awarded Dean's Teaching Commendation
	CS 7940	HWRT Seminar	2	
	CS/ECE 3991	Computer Engineering Jr. Seminar	14	
Spring 09	CS/ECE 5830	VLSI Architecture	29	
	CS/ECE 6830	VLSI Archticture	9	
Fall 08	CS/ECE 3710	Computer Design Lab	38	Awarded Dean's Teaching Commendation
	CS 7940	HWRT Seminar	2	
Spring 08	CS/ECE 3700	Digital System Design	118	
	CS/ECE 6712	Digital IC Testing	12	
Fall 07	CS/ECE 5710	Digital VLSI	20	Awarded Dean's Teaching Commendation
	CS/ECE 6710	Digital VLSI	30	Awarded Dean's Teaching Commendation
	CS/Art 5965/6965	Special Topics: VLSI and Art	5	
	CS 7940	HWRT Seminar	4	
Spring 07	CS/ECE 6830	VLSI Architecture	12	Awarded Dean's Teaching Commendation
	CS/ECE 5830	VLSI Architecture	3	Awarded Dean's Teaching Commendation
	CS/ECE 6712	Digital VLSI Testing	11	
	CS 6967	ST-Multithreaded Architecture	6	
Fall 06	CS/ECE 6710	Digital VLSI	50	
	CS 7940	HWRT Seminar	6	
Spring 06		Asynchronous Circuits	24	At Columbia Univ, NYC on Sabbatical
Fall 05	none	Sabbatical Leave		
Spring 05	CS/EE 6830	VLSI Architecture	19	
	CS 6967	VLSI Testing	8	
Fall 04	CS/EE 5710	Digital VLSI	19	Awarded Dean's Teaching Commendation
	CS/EE 6710	Digital VLSI	32	Awarded Dean's Teaching Commendation
	CE/EE 6900	Architecture Seminar	3	

Date	Course Number	Course Name	Class Size	Comments
Spring 04	CS/EE 5830	VLSI Architecture	12	Awarded Dean's Teaching Commendation
	CS/EE 6830	VLSI Architecture	14	Awarded Dean's Teaching Commendation
	CS/EE 6967	VLSI Testing	5	
Fall 03	CE/EE 5710	Digital VLSI	18	
	CE/EE 6710	Digital VLSI	38	
	CE/EE 6900	Architecture Seminar	3	
Spring 03	CS/EE 5830	VLSI Architecture	10	
	CS/EE 6830	VLSI Architecture	12	
	CS/EE 6967	VLSI Testing	5	
Fall 02	CS/EE 3710	Computer Design Lab	49	
	CS/EE 5710	Digital VLSI Design	15	
	CS/EE 6710	Digital VLSI Design	43	
Spring 02	CS 5964/6964	VLSI Testing	6	
	CS 6943	Asynchronous Seminar	14	Awarded Dean's Teaching Commendation
	CS/EE 3700	Digital System Design	135	Awarded Dean's Teaching Commendation
Fall 01	CS/EE 5710	Advanced I.C. Design I	33	
	CS/EE 6710	Advanced I.C. Design I	27	
Spring 01	CS/EE 5830	VLSI Architecture	25	Awarded Dean's Teaching Commendation
	CS/EE 6830	VLSI Architecture	13	
Fall 00	CS/EE 3710	Computer Design Lab	43	Awarded Dean's Teaching Commendation
	CS/EE 5810	Adv. Computer Architecture	16	
	CS/EE 6810	Adv. Computer Architecture	46	
Spring 00	CS/EE 3700	Digital System Design	130	
	CS 4500	Software Engineering	75	Team-taught with Kessler & Henderson
Fall 99	CS/EE 5810	Adv. Computer Architecture	6	
	CS/EE 6810	Adv. Computer Architecture	26	
Spring 99	None	On Sabbatical		at University of Manchester, England
Fall 98	CSE467	Adv. Digital Logic	24	U of Washington, Seattle during sabbatical
Spring 98	CS367	Computer Design Lab	43	Awarded Dean's Teaching Commendation
Winter 98	CS568	VLSI Architecture	15	Awarded Dean's Teaching Commendation
	CS682	ASIC Seminar (with Ganesh)	3	
Autumn 97	CS361	Hardware Fundamentals	104	Awarded Dean's Teaching Commendation
	CS685	ASIC Seminar (with Ganesh)	2	
Spring 97	CS367	Computer Design Lab	26	Awarded Dean's Teaching Commendation
Winter 97	CS568	VLSI Architecture	17	
	CS685	ASIC Seminar	2	
Autumn 96	CS361	Hardware Fundamentals	108	Awarded Dean's Teaching Commendation
	CS685	ASIC Seminar (with Ganesh)	2	

Top 15% cutoff and median values are based on scores from all classes taught in the College of Engineering.

Date	Course Number	Course Name	Class Size	Evaluation Results	Top 15% Cutoff	Median
Spring 96	CS367	Computer Design Lab	40	1.11	1.11	0.30
	CS682	ASIC Seminar (with Ganesh)	5			
Winter 96	CS568	VLSI Architecture	15	0.61	1.13	0.45
	CS685	Async Seminar	2			
Autumn 95	CS361	Hardware Fundamentals	85	0.70	1.12	0.23
	CS685	ASIC Seminar (with Ganesh)	2			
Spring 95	CS572	High Level Synthesis: VHDL	21	0.69	1.18	0.41
	CS682	ASIC Seminar (with Ganesh)	5			
	CS685	Async Seminar	1			
Winter 95	CS365	Hardware Fundamentals	86	0.87	1.20	0.45
	CS682	ASIC Seminar (with Ganesh)	2			
	CS685	Async Seminar	5			
Autumn 94	CS568	VLSI Architecture	10	1.62	1.00	.39
	CS685	ASIC Seminar (with Ganesh)	2			
Spring 94	CS544	Advanced VLSI Design	14	1.26	1.13	.32
	CS545	Testing Integrated Circuits	5	Evaluated with CS544		
	CS682	ASIC Seminar (with Ganesh)	4			
	CS685	Async Seminar	1			
Winter 94	CS365	Hardware Fundamentals	91	.91	1.17	.29
	CS682	ASIC Seminar (with Ganesh)	4			
	CS685	Async Seminar	1			
Autumn 93	CS568	VLSI Architecture	12	1.25	1.14	.21
	CS685	ASIC Seminar (with Ganesh)				
Spring 93	CS562	Parallel Computer Organization	7	.25	1.12	.32
	CS682	ASIC Seminar (with Ganesh)	2			
	CS685	Async Seminar	3			
Winter 93	CS365	Hardware Fundamentals	87	1.33	1.22	.36
	CS682	ASIC Seminar (with Ganesh)	1			
	CS685	Async Seminar	5			
Autumn 92	CS571	VLSI Architecture	15	1.12	1.12	.36
	CS682	ASIC Seminar (with Ganesh)				
Spring 92	CS562	Parallel Computer Organization	10	1.05	1.01	.25
	CS682	ASIC Seminar (with Ganesh)	3			
	CS685	NSR Seminar	3			
Winter 92	CS561	Adv. Computer Organization	31	.88	1.16	.18
	CS682	ASIC Seminar (with Ganesh)	5			
Autumn 91	CS572	VLSI Architecture	14	Results lost by Dean's office		
	CS682	ASIC Seminar (with Ganesh)	2			
Spring 91	CS562	Parallel Computer Organization	6	.47	1.24	.30
	CS682	ASIC Seminar (with Ganesh)	3			
Winter 91	CS561	Adv. Computer Organization	26	.71	1.1	.42
	CS684	ASIC Seminar (with Ganesh)	5			
Autumn 90	CS572	VLSI Architecture	10	1.05	1.07	.28
	CS682	ASIC Seminar (with Ganesh)	2			

Teaching-Related Grants & Gifts

Title:	University Professorship
Agency:	Undergraduate College, University of Utah
Total Award:	$35,000 ($20,000 for class development, $10,000 to department for support of teaching relief, $5,000 individual award)
Duration:	Fall 2014-Spring 2016
Principal Investigator:	Erik Brunvand

Title:	The Big Draw: Art and Engineering Collaboration in Automated Drawing
Agency:	Council of Dee Fellows, University of Utah
Total Award:	$8400
Duration:	Fall 2011-Spring 2012
Principal Investigator:	Erik Brunvand
Co-Principal Investigator:	Paul Stout, Department of Art and Art History

Title:	University Teaching Assistantship
Agency:	Graduate School, University of Utah
Total Award:	$15,000
Duration:	Fall 2010 - Spring 2011
Principal Investigator:	Erik Brunvand
Notes:	Support for Josef Spjut as a UTA

Title:	Embedded Systems and Kinetic Art
Agency:	University of Utah Teaching Committee
Total Award:	$4,300
Duration:	Received September 2009
Principal Investigator:	Erik Brunvand
Co-Principal Investigator:	Paul Stout, Department of Art and Art History

Title:	IODrive 160GB solid state memory card
Agency:	FusionIO Inc.
Total Award:	Equipment worth $6,570
Duration:	Received September 2009
Principal Investigator:	Erik Brunvand
Co-Principal Investigator:	Dave Nellans, graduate student

Title:	Xilinx Educational Donation (Gift of Xilinx prototyping boards)
Agency:	Xilinx Inc.
Total Award:	Equipment worth$4,200
Duration:	Received March 2009
Principal Investigator:	Erik Brunvand

Title:	Engineering/Art Collaborative Course
Agency:	University of Utah Teaching Committee
Total Award:	$7,075
Duration:	Received September 2007
Principal Investigator:	Erik Brunvand
Co-Principal Investigator:	Justin Diggle, Department of Art and Art History

Title:	Xilinx Educational Donation (Gift of Xilinx prototyping boards for evaluation)
Agency:	Xilinx Inc.
Total Award:	Equipment worth $2,493
Duration:	Received September 2006
Principal Investigator:	Erik Brunvand

Title:	John R. Park Teacher's Fellowship
Agency:	University of Utah
Total Award:	$10,000
Granted:	Spring 2005
Principal Investigator:	Erik Brunvand

Title:	University Teaching Assistantship
Agency:	Graduate School, University of Utah
Total Award:	$11,000
Granted:	Fall 2004
Principal Investigator:	Erik Brunvand
Notes:	Support for Vamshi Kadaru as a UTA

Title:	Computer Engineering Lab Enhancement
Agency:	Governor's Initiative in Engineering
Total Award:	$110,000
Granted:	September 2001
Principal Investigator:	Erik Brunvand

Courses Developed

UGS/CS 2050 — As part of my University Professorship I am developing a new undergraduate course on the theme of *technological fluency*. This course will be offered (at least) during the Spring semesters in 2015 and 2016 as part of the General Education program. This course, titled Making Noise: Sound Art and Digital Media, will introduce students from across campus to a variety of digital media subjects that also involve computation. I plan to emphasize hands-on projects that include both programming and physical/electronic artifacts. Essentially this is a way to introduce students to computing and increase their technological fluency but through digital media projects rather than engineering projects. It is also a way to expand students ideas about technology in the arts and how arts and technology interact in our modern world. This will be a lower-division course that will serve a variety of General Education purposes, and will culminate with a public presentation of student projects.

CS6965/6958 — Hardware Ray Tracing — A special topics class first taught in Fall 2012, and again in Spring 2014, and Spring 2015 (offered in 2015 by my graduate students, Daniel Kopta and Konstantin Shkurko), this class explores ray tracing as a commuter graphics rending technique and how the algorithm interacts with special purpose hardware. Students implement ray tracing software and run that application on a simulation of a special-purpose architecture for graphics processing developed by my research group. Through this exploration students get experience not only with the practice of computer architecture research, but first-hand experience in proposing architectural changes to support specific algorithms.

CS5789 — Embedded Systems and Kinetic Art — First taught in the fall of 2009, this course was developed as a collaborative course with Professor Paul Stout in the Department of Art and Art History. The aim is to pair embedded systems students (mostly Computer Science and Computer Engineering students) with Art students (mostly sculpture majors) to make kinetic art projects. Kinetic art is art that uses motion, light, or sound as part of its realization. In practice many kinetic art projects use microcontrollers to control the kinetic aspect of the art. The aim of this class is to enhance the creative problem solving skills of the engineers, and the engineering skills of the artists through the group projects.

CS/Art 5965/6965 — VLSI and Art — A special topics course taught in the Fall of 2007, this course was developed as a cooperative course with Professor Justin Diggle in the Department of Art and Art History. The plan was to get artists (printmakers in particular) together with engineers (VLSI chip designers in particular) to do joint projects involving integrated circuits and art. A Teaching Committee grant was received for this collaborative course for $7075 which was used to buy a large format printer to support the course.

CS 6967 — Multithreaded Computer Architecture — A special topics course in Spring 2007. This is a project-based special topics course to study multithreaded approaches to computer architecture. This course led to the architectural simulation infrastructure that we are still using in my Hardware Ray Tracing research group.

CS/EE 5830/6830 — VLSI Architecture — This is a new course from Spring 2005 on digital computer arithmetic. It was developed from the ground up to study high-performance arithmetic circuits in detail.

CS/EE 6712 — Digital VLSI Testing — A course where students test the chips that they designed in 5710/6710. Because students can fabricate their chips in 5710/6710, a course is needed in the spring in order to test those chips. We use the dedicated LV500 test hardware for this lab class.

CS/EE 5710/6710 — Digital VLSI Design — After Prof. Kent Smith's retirement in spring 2001, I took over this course and completely restructured it. This course now involves a major project, uses CAD tools from Cadence and Synopsys, and has a strong emphasis on building large VLSI systems. It also allows students to fabricate their projects as integrated circuits.

During my sabbatical in Spring 2006 I wrote the first draft of a new VLSI CAD Manual textbook for this course. I

used the draft in my Fall 2006 offering of the course, and am revising it based on that experience. I am currently in discussions with Addison Wesley about publication.

CS/EE 5810/6810 — Restructured this Advanced Computer Architecture course in the Fall of 2000 to use a lab-based approach where students build a timing simulator of a pipelined, out-of-order, branch predicting machine along with the discussions in the book.

CS4500 — Senior Software Lab — Bob Kessler, Tom Henderson, and I restructured this course in Spring 2000 to be a project-driven course with individual group meetings rather than lectures. We also included a design contest with judges and prizes from local companies. The result was a great success.

CS361-2-3 (Now CS3700-3810)— Digital Logic — Helped restructure the sophomore digital logic sequence. This sequence was formerly numbered 364-5-6. The sequence has been changed to be bottom-up starting with digital design in the fall, and moving up to computer systems in the spring. A new book was used, and the curriculum has been changeed to be consistant across the three classes in the sequence. This change allows students to build much more significant circuit projects than in the past because they start building circuits in the fall, and continue through spring. In the older version the lab kits were used only in winter and spring quarters.

CS367 (Now CS3710) — Computer Design Lab — Redesigned the sophmore digital design lab course to involve designing and building a realistic computer processor. Xilinx and Actel FPGA are used so that the students can build designs that are much larger, more realistic, and complex than previously possible in this class.

CS365 — Restructured the basic digital logic class around the use of new commercial CAD tools from VIEW*logic* and also introduced Xilinx FPGAs into the lab portion of the class. The entire 300-level hardware series will be restructured starting in Fall 1995 using a bottom-up approach starting with digital logic in the fall, and ending with the hardware/software interface in the spring.

Special Topics, VHDL — This course was developed to teach high-level hardware synthesis using the VHDL language. This is an industry standard hardware description language and is used through the VIEW*logic* tools, and other new CAD tools now available to our classes. It was developed as part of the Advanced VLSI course taught in Spring 1994. It was taught again as a special topics course in Spring 1995.

CS568 (now CS/EE 5830/6830) — Developed a new course to let students investigate the mapping of computer architecture into VLSI through the use of Field Programmable Gate Arrays (FPGAs). Students design VLSI systems and implement them in the same quarter using Actel FPGA technology.

CS561 — Designed course around a new book (Hennessey and Patterson, Computer Architecture: A Quantitative Approach). This course emphasizes quantitative aspects of computer architecture by using measurements of machine usage as a guide to developing advanced computer architectures.

CS562 — Developed course to teach students about the architecture of parallel machines. Case studies of existing parallel computers are used to illustrate different design decisions.

Async Seminar — This seminar course allows students to explore individual ideas related to asynchronous circuits and systems.

Service

Professional Activities

Referee for:

- ACM SIGGRAPH
- ACM SIGCSE
- High Performance Graphics conference
- Great Lakes Symposium on VLSI
- IEEE Symposium on Asynchronous Circuits and Systems
- Impact printmaking conference
- Proceedings of the IEEE
- Formal Methods in System Design
- Harper Collins
- IEEE Design and Test of Computers
- IEEE Transactions on Computers
- IEEE Transactions on Computer Aided Design
- IEEE Transactions on VLSI
- IEE Journal on Computers and Digital Techniques
- International Journal of Parallel Programming
- Journal of VLSI Signal Processing
- Klewer Academic Publishers
- National Science Foundation (1-2 panels per year on average)
- National Conference on Undergraduate Research (All C.S. related submissions for the 1993 conference).
- Prentice-Hall
- And others I've forgotten about...

Conferences:

ACM SIGGRAPH Education Chair, 2017, 2018

General co-Chair of the 2012 ACM Great Lakes Symposium on VLSI (GLSVLSI), Salt Lake City, UT, May 2012.

General Chair of the 2011 IEEE International Symposium on Asynchronous Circuits and Systems (Async 2011) held in Ithaca, New York in April 2011

Technical Program co-Chair of the Great Lakes Symposium on VLSI (GLSVLSI) 2010.

General Chair of the 2001 IEEE International Symposium on Asynchronous Circuits and Systems (Async 2001) held in Salt Lake City in March, 2001.

General Chair and co-Program Chair (with Chris Myers) of the 2001 Conference on Advanced Research on VLSI, held in Salt Lake City in March, 2001.

Steering Committee for the IEEE International Symposium on Asynchronous Circuits and Systems, Chair 1994 — 2008. Member 2008 — present.

Steering Committee for ACM Great Lakes Symposium on VLSI (GLSVLSI), 2012 — present.

Member of the program committee for the IEEE International Symposium on Asynchronous Circuits and Systems, 1994, 1996, 1997, 1998, 1999, 2000, 2003, 2004, 2005, 2006, 2007, 2009, 2010, 2012, 2013, 2014, 2015, 2016, 2017.

Publication chair for the International Symposium on Advanced Research in Asynchronous Circuits and Systems 1997, 1998, 2000, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018.

Publication Chair for the 2008 High Performance Computer Architecture (HPCA) conference to be held in Salt Lake City.

Member of Program Committee for ACM/Eurographics High Performance Graphics, 2009, 2010, 2011, 2012, 2013, 2014.

Member of Program Committee for IEEE Symposium on Interactive Ray Tracing (RT), 2006, 2007, 2008.

Member of the program committee for the ACM Great Lakes Conference on VLSI (GLSVLSI), 2003, 2005, 2006 (track co-chair), 2009 (track co-chair).

NSF research funding Panels, November 1997, October 2000, May 2001, October 2001, September 2004, September 2005, September 2006, September 2007, July 2009, September 2009, April 2010, March 2012, March 2013, May 2014, October 2014, March 2015.

Member of the program committee for the 20th Anniversary Conference on Advanced Research in VLSI, Georgia Institute of Technology, March 1999.

Member of the program committee for the IEEE International Conference on Computer Design (ICCD) 1995, 1996, 1997.

U.S. academic representative for the 1996 International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async96), Aizu, Japan, March 1996.

Organizer and Co-General Chair (with Al Davis) for the 1994 International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async94), held in Salt Lake City in November 1994.

Member of the program committee for the 6th NASA Symposium on VLSI, Albuquerque, New Mexico, January 1995.

Coordinator (with Ganesh Gopalakrishnan) of a day-long "minitrack" on asynchronous circuits and systems, 26th Hawaii International Conference on System Sciences, January 5-8, 1993.

Member of the program committee for the International Workshop on Field Programmable Logic and Applications:

— 1993, Oxford University, England
— 1994, Prague, The Czech Republic
— 1995, Oxford University, England

Honors and Awards

Awarded two-year University Professorship from the Undergraduate College for the academic years 2014-2015 and 2015-2016.

Awarded School of Computing Outstanding Teaching Award, 2012.

Best Paper award for "TRaX: A multi-threaded architecture for real-time ray tracing," by J. Spjut, D. Kopta, S. Boulos, S. Kellis, and E. Brunvand. In *6th IEEE Symposium on Application Specific Processors (SASP)*, June 2008.

Awarded a John R. Park Fellowship from the University of Utah for $10,000 to support teaching-related activities while on sabbatical in 2005/2006. $5000 is to me, and $5000 to the department to support teaching in my absense.

Awarded the University Distinguished Teaching Award, 2002-2003, University of Utah (also nominated in 2001-2002).

Nominated for Utah Engineers Council, Utah Engineering Educator of the Year award, 2003.

College of Engineering Outstanding Teaching Award for 1997, University of Utah, College of Engineering.

Best Paper Award for "Precise Exception Handling for a Self-Timed Processor," by William Richardson and Erik Brunvand. in International Conference on Computer Design (ICCD95), October 1995, Austin TX.

External examiner for Richard G. Burford (M.S. 1995), "Asynchronous Logic Building Blocks for Pipelined DSP Applications," from The Flinders University of South Australia. Neil Bergman, Committee Chair.

External examiner for Sven Woop (Ph.D. 2007), "DRPU: Hardware for Dynamic Interactive Ray Tracing," from Saarland University, Saarbruecken, Germany. Philipp Slusallek, Committee Chair.

First place in Design Methodologies Division, Actel Design Contest 1991, "Self-Timed Design using Actel FPGAs."

University Academic Committees

University Teaching Committee, Chair 2015 to present, Chair, 2001–2005, member 1999–2001, and 2013–2014.

Graduate School Review Committee for the Department of Film and Media Studies, 2014.

Creative Campus Steering Committee, 2012–present

University Research Committee, 2006–2009

University Conflict of Interest Committee, 2000–2002.

Bachelor of University Studies Committee, 1996–1998.

Graduate School Review Committee for the Department of Parks, Recreation and Tourism, 1997.

University of Utah Faculty Club:

— President 1995-1996
— Vice President 1994-1995
— Treasurer 2008–present.
— Member of the Board of Directors, 1992–1994, 1999, 2000, 2001-2005, 2006–2014.

College of Engineering Academic Committees

Curriculum Committee, 2011–present.

ABET Committee, 2006–present.

Director of the Computer Engineering Program (an ABET-accredited BS degree granting program in the College of Engineering), 1993–1997, 2002–2005, 2009–2012, 2015–present.

RPT Committee, 1999–2001.

Computing Committee, 1999–2000.

Chair of Academic Appeals Committee, 1998–1999.

College Council, 1991–1994.

Departmental Academic Committees

Director of Computing Degree Track in Computer Engineering, 2007–present

Director of Computing Degree Track in Digital Media, 2011–2015 (track put on hiatus)

Member, HCC Track Faculty 2017 – present

Director of Graduate Studies. 1997–1998, 2007–2009

Director of Graduate Admissions, 1995–1997, 2006–2007

Curriculum Committee, 2011–present.

Scholarship Committee, 2014–present.

Graduate Admissions Committee, 1999–2000, 2008–present.

Department RPT Chair, 2001–2003.

Chair of Computing Policy Committee, 1999–2000.

Graduate Studies Committee, 1995–1996, 2006–2007, 2010–present.

Semester Conversion Committee, 1997–1998.

Computer Engineering Committee

— Chair, 1993–1997, 2002–2005, 2009–2012
— Member, 1992–1993, 1999–2002, 2006–2009, 2012–present

Chair of Hardware Comprehensive Exam Committee, 1999, 2000.

Member, Graduate Comprehensive Exam Commitee, 1996, 1998, 2001, 2002.

Faculty Recruiting Committee, 1992 — 1993.