Erik Brunvand

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EDUCATION

Carnegie Mellon University — **Pittsburgh, PA**
PhD, Computer Science — *1991*
Dissertation title: Translating Concurrent Communicating Programs into Asynchronous Circuits

University of Utah — **Salt Lake City, UT**
MS, Computer Science — *1984*
Thesis title: Context Addressable Memory for Symbolic Processing Systems
BS, Computer Science & BS, Mathematics (Magna cum Laude) — *1982*

PROFESSIONAL EMPLOYMENT

Current

University of Utah — **Salt Lake City, UT**
- Professor of Computer Science, Kahlert School of Computing — *1990–Present*
  (Assistant Professor from 1990-1996, Associate Professor from 1997-2020)
- Adjunct Professor of Electrical and Computer Engineering — *1999–Present*

National Science Foundation — **Alexandria, VA**
- Program Director, CISE/CNS/CSR *(Computer Systems Research)* — *2019-2024*
  Full time 2019-2022, and continuing part-time through August 2024)

Previous

University of Utah — **Salt Lake City, UT**
- University Professor - honorary rank from the Office of Undergraduate Studies — *2014–2016*
- Director, Computer Engineering Program, College of Engineering — *2002–2005, 2009–2012, 2015–2018*

University of Washington — **Seattle, WA**
- Visiting Professor, DXARTS Program — *Fall, 2012*

Columbia University — **New York, NY**
- Visiting Professor, CS Department — *Spring 2006*

Max Planck Institut für Informatik, University of Saarland — **Saarland, Germany**
- Visiting Professor, CS Department — *Fall 2005*

University of Manchester — **Manchester, UK**
- Visiting Professor, School of Computer Science — *Spring 1999*

University of Washington — **Seattle, WA**
- Visiting Professor, CSE Department — *Fall 1998*

Carnegie Mellon University — **Pittsburgh, PA**
- Research Assistant, CS Department — *1984–1990*

Sutherland, Sproull & Associates — **Pittsburgh, PA**
- Research Assistant — *1986–1987*

SCHOLARSHIP

Publications — Books

1. Erik Brunvand, *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools*, *Addison-Wesley, 2010. ISBN:0321547993 9780321547996*

Publications — Refereed Journals — Student authors are underlined

0. K. Shkurko, T. Grant, D. Kopta, I. Mallett, E. Vasiou, C. Yuksel, E. Brunvand, "Analysis of Dual Streaming for Hardware-Accelerated Ray Tracing," *Submitted to IEEE Transactions on Visualization and Computer Graphics (TVCG).*
1. A. Banerjee, S. Basu, E. Brunvand, P. Mazumder, W. R. Cleaveland II, G. Singh, M. Martonosi, F. Pembleton, "Navigating the Seismic Shift of Post-Moore Computer Systems Design," *IEEE Micro*, Vol 41, n6, 2021. `https://10.1109/MM.2021.3114899`
2. S Basu, E. Brunvand, "Semiconductor Microelectronic Research at NSF/CISE: Status and Challenges," IEEE VLSI Circuits and Systems Letters, Vol 7, Issue 2, Feb 2021.
3. E. Vasiou, K. Shkurko, E. Brunvand, C. Yuksel, "Mach-RT: A Many Chip Architecture for High Performance Ray Tracing," *IEEE Transactions on Visualization and Computer Graphics (TVCG), 2020.*
4. E. Brunvand and W. Wischer, "Collective Currents: Exploring Sustainability through a Collaborative and Interactive Installation," Leonardo, Vol 54, N3, 2021. `https://doi.org/10.1162/leon_a_01880`
5. E. Vasiou, K. Shkurko, I. Mallett, E. Brunvand, C. Yuksel, "A Detailed Study of Ray Tracing Performance: Render Time and Energy Cost," The Visual Computer, Vol 34, Issue 6–8, June 2018. `https://doi.org/10.1007/s00371-018-1532-8`
6. K. Shkurko, C. Yuksel, D. Kopta, I. Mallett, E. Brunvand, "Time Interval Ray Tracing for Motion Blur," IEEE Transactions on Visualization and Computer Graphics, Vol 24, Issue 12, Nov 2017. `https://doi.org/10.1109/TVCG.2017.2775241`
7. E. Brunvand and N. McCurdy, "Making Noise: Sound Art for Exploring Technology Fluency," ACM Inroads, Vol 8, No 2, June 2017. `http://doi.acm.org/10.1145/3095781.3017714`
8. D. Kopta, K. Shkurko, J. Spjut, E. Brunvand, A. Davis. "Memory Considerations for Low-Energy Ray Tracing," Computer Graphics Forum, Vol 34, No. 1, Feb 2015. `https://doi.org/10.1111/cgf.12458`
9. E. Brunvand, "Speculatorum Oculi," Leonardo, Vol 47, No. 4, Aug 2014. `https://doi.org/10.1162/LEON_a_00856`
10. E. Brunvand and A, Denyer, "Micro-Scale Printmaking on Silicon," Leonardo, Vol 44, No. 5, Sept/Oct 2011. `https://doi.org/10.1162/LEON_a_00238`
11. D. Nellans, K. Sudan, E. Brunvand, R. Balasubramonian, "Improving Server Performance on Multi-Cores via Selective Off-loading of OS Functionality, LNCS 2010. `https://doi.org/10.1007/978-3-642-24322-6_23`
12. Josef Spjut, Andrew Kensler, Daniel Kopta, Erik Brunvand, "TRaX:, A Multicore Hardware Architecture for Real-Time Ray Tracing," IEEE Transacations on CAD, Vol 28, n12, Dec 2009. `https://doi.org/10.1109/TCAD.2009.2028981`
13. David Nellans, Rajeev Balasubramonian, Erik Brunvand, "OS Execution on Multi-Cores: Is Out-Sourcing Worthwhile?" ACM Operating Systems Review, Vol 43, No. 2, April 2009. `https://doi.org/10.1145/1531793.1531812`
14. P. Shirley, K. Sung, E. Brunvand, A. Davis, S. Parker, S. Boulos, "Fast ray tracing and the potential effects on graphics and gaming courses," Computers & Graphics 32 (2), 2008. `https://doi.org/10.1016/j.cag.2008.01.007`
15. Ganesh Gopalakrishnan, Prabhakar Kudva, Erik Brunvand, "Peephole Optimization of Asynchronous Macro-module Networks," IEEE Transactions on VLSI Systems, Vol. 7, No. 1, March 1999. `https://doi.org/10.1109/92.748198`
16. William Richardson and Erik Brunvand, "Architectural Considerations for a Self-Timed Decoupled Processor,"

IEE Proceedings on Computers and Digital Techniques, Special issue on Asynchronous Processors. Vol. 143, No. 5, September 1996. https://doi.org/10.1109/ASYNC.1996.494438

17. V. Chandramouli, Erik Brunvand, Kent Smith, "Self-Timed Design in GaAs - Case Study of a High-Speed Parallel Multiplier," *IEEE Transactions on VLSI Systems*, March 1996. https://doi.org/10.1109/TVLSI.1996.486090
18. Ganesh Gopalakrishnan, Erik Brunvand, Nick Michell, Steve Nowick, "A Correctness Criterion for Asynchronous Circuit Validation and Optimization", *IEEE Transactions on Computer Aided Design* V13, n11, November 1994. https://doi.org/10.1109/43.329261
19. Erik Brunvand, "Designing Self-Timed Systems using Concurrent Programs," *Journal of VLSI Signal Processing*, 7, 1994, Special issue on asynchronous systems. https://doi.org/10.1007/978-1-4615-2794-7_5
20. Erik Brunvand, "Using FPGAs to Implement Self-Timed Systems," *Journal of VLSI Signal Processing*, 6, 1993, Special issue on FPGAs. https://doi.org/10.1007/BF01607880

Guest Editor of Journals

1. Erik Brunvand, Steve Furber, and Takashi Nanya eds., Special issue on Asynchronous Computer Architecture, *IEE Journal on Computers and Digital Techniques*. Special issue on Asynchronous Processors. Vol. 143, No. 5, September 1996.
2. Erik Brunvand, Ganesh Gopalakrishnan eds., Special issue on asynchronous circuits and systems, *Integration: The VLSI Journal*. vol 15 (1993).

Publications — In Books — Student authors are underlined

1. Erik Brunvand, "Adding Bling: Using LEDs with Arduino," In: M. Majid al-Rifaie, A. Ursyn, and T. Wyeld "The Art of Coding: The Language of Drawing, Graphics, and Animation." CC Press, Boca Raton, FL 2020.
2. John Hurdle, Erik Brunvand, and Lüli Josephson, "Asynchronous VLSI Design for Neural System Implementation," In: Delgado-Frias J.G., Moore W.R. (eds) "VLSI for Neural Networks and Artificial Intelligence." Springer, Boston, MA 1995. ISBN 978-1-4899-1331-9
3. John Hurdle, Lüli Josephson, and Erik Brunvand, "Reliable Interfacing of Self-Timed FPGA-based Neural Classifiers to Synchronous Parts," In "More FPGAs" Abingdon EE&CS Books, Abington, England 1994, Will R. Moore and Wayne Luk, Editors. ISBN: 0951845314
4. Erik Brunvand, "Windchime: An FPGA-based Self-Timed Parallel Processor," In "More FPGAs" Abingdon EE&CS Books, Abington, England 1994, Will R. Moore and Wayne Luk, Editors. ISBN: 0951845314
5. Erik Brunvand, "Implementing Self-Timed Systems with FPGAs", In "FPGAs" Abingdon EE&CS Books, Abington, England 1991, Will R. Moore and Wayne Luk, Editors. ISBN: 0951845306

Publications — Refereed Conferences — Student authors are underlined

1. D. Lin, E. Vasiou, C. Yulsel, D. Kopta, E. Brunvand, "Hardware-Acclerated Dual-Split Trees," in High Performance Computer Graphics (HPG 2020), Virtual Event, July 2020. *(ACM DL pending ...)*
2. E. Vasiou, K. Shkurko, E. Brunvand, C. Yuksel, "Mach-RT: A Many Chip Architecture for Ray Tracing," in High-Performance Computer Graphics (HPG 2019), Strasbourg, France, July 2019. *(ACM DL pending ...)*
3. E. Brunvand, "Extending Student Labs with SMT Circuit Implementation," Great Lakes Symposium on VLSI (GLSVLSI 2019), Washington, D.C., May, 2019. https://doi.org/10.1145/3299874.3317968
4. E. Brunvand, D. Kline, A. Jones, "Dark Silicon Considered Harmful: A Case for Truly Green Computing," International Green and Sustainable Computing Conference (IGSC), Pittsburgh, PA, Oct 2018. ***Awarded Best Paper at IGSC'18*** *(IEEE Xplore pending ...)*
5. K. Shkurko, T. Grant, E. Brunvand, D. Kopta, J. Spjut, E. Vasiou, I. Mallett, C. Yuksel, "SimTRaX: Simulation Infrastructure for Exploring Thousands of Cores," Great Lakes Symposium on VLSI (GLSVLSI 2018), Chicago, Illinois, 2018. https://doi.org/10.1145/3194554.3194650

6. E. Brunvand and D. Kopta, "Power and Energy Implications of Misunderstanding DRAM," International Green and Sustainable Computing Conference (IGSC), Orlando, FL, Oct, 2017. https://doi.org/10.1109/IGCC.2017.8323589
7. D. Kline, N. Parshook, A. Johnson, J. Stine, W. Stanchina, E. Brunvand and A. Jones, "Sustainable IC Design and Fabrication," International Green and Sustainable Computing Conference (IGSC), Orlando, FL, Oct, 2017. https://doi.org/10.1109/IGCC.2017.8323572
8. K. Shkurko, T. Grant , D. Kopta, I. Mallett, C. Yuksel, E. Brunvand, "Dual Streaming for Hardware-Accelerated Ray Tracing," in High-Performance Computer Graphics (HPG 2017), Los Angeles, CA, July 2017. https://doi.org/10.1145/3105762.3105771
9. E. Brunvand and N. McCurdy, "Making Noise: Using Sound-Art to explore Technological Fluency," ACM SIGCSE, Seattle, WA, 2017. https://doi.org/10.1145/3095781.3017714
   Awarded Best Paper at SIGCSE 2017
   (re-presented also at ACM SIGGRAPH 2017, Los Angeles, as part of the "SIGCSE Reprise at SIGGRAPH 2017," http://s2017.siggraph.org/educators-forum.html)
10. D. Kline, N. Parshook, X. Ge, E. Brunvand, R. Melhem, P. Chrysanthis and A. Jones, "Holistically Evaluating the Environmental Impacts in Modern Computing Systems," International Sustainable and Green Computing (ICSG) Conference, Hangzhou, China, Nov 2016. https://doi.org/10.1109/IGCC.2016.7892605
11. J G Alford and Erik Brunvand, "Leveraging CS Teachable Moments in the Maker Movement," ACM SIGCSE, Memphis, TN, 2016. https://doi.org/10.1145/2839509.2850497
12. E. Brunvand, "A Noise-Based Curriculum for Technological Fluency," ACM SIGGRAPH 2015, Los Angeles, CA, August 2015. https://doi.org/10.1145/2785585.2792548
13. Erik Brunvand, "Computational Thinking Meets Design Thinking: Technology and Arts Collaborations." In Great Lakes Symposium on VLSI (GLSVLSI '15). Pittsburgh, PA. https://doi.org/10.1145/2742060.2742123
14. E. Brunvand, "Using Surface-Mount Components in an Embedded Systems Lab," ACM Workshop on Computer Architecture Education (WCAE), Portland, OR, June 2015. https://doi.org/10.1145/2795122.2795129
15. E. Brunvand, "Technological Fluency through Circuit Bending," International Conference on Microelectronic Systems Education, Pittsburgh, PA, May 2015. https://doi.org/10.1109/MSE.2015.7160012
16. E. Brunvand, N. Chatterjee, D. Kopta, "Why Graphics Programmers Need to Know about DRAM," in *ACM SIGGRAPH 2014 Courses*, SIGGRAPH 2014, Vancouver, B.C., Canada. https://doi.org/10.1145/2614028.2615421
17. Daniel Kopta, Konstantin Shkurko, Josef Spjut, Erik Brunvand, Al Davis, "An Energy and Bandwidth Efficient Ray Tracing Architecture," in High-Performance Computer Graphics (HPG 2013), July 2013. https://doi.org/10.1145/2492045.2492058
18. Erik Brunvand, "Lights! Speed! Action!: Fundamentals of physical computing for programmers," in *ACM SIGGRAPH 2013 Courses*, SIGGRAPH '13, (New York, NY, USA), pp. 13:1–13:108, ACM, 2013. https://doi.org/10.1145/2504435.2504448
19. Erik Brunvand, "Arts/tech collaboration with embedded systems and kinetic art," SIGGRAPH '13, (New York, NY, USA), ACM, 2013. https://doi.org/10.1145/2504459.2504488
20. E. Brunvand, J. G. Alford, and P. Stout, "Drawing machines: Exploring embedded system programming and hardware with an artistic flair," SIGCSE, Denver, CO, ACM, 2013. https://doi.org/10.1145/2445196.2445530
21. Daniel Kopta, Thiago Ize, Josef Spjut, Erik Brunvand, Al Davis, Andrew Kensler, "Fast, Effective BVH Updates for Animated Scenes," ACM SIGGRAPH Symposium on Interactive 3D Graphics and Games (I3D), Mar, 2012. https://doi.org/10.1145/2159616.2159649
22. Joseph Spjut, Daniel Kopta, Erik Brunvand, Al Davis, "A Mobile Accelerator Architecture for Ray Tracing," 3rd Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW-3), Feb 2012. http://www.ece.lsu.edu/hpca-18/shaw-3/
23. E. Brunvand, "Games as Motivation in Computer Design Courses: I/O is the Key," SIGCSE, Dallas, ACM, March 2011. https://doi.org/10.1145/1953163.1953178

24. E. Brunvand, P. Stout, "Kinetic Art and Embedded Systems: A Natural Collaboration," SIGCSE, Dallas, ACM, March 2011. https://doi.org/10.1145/1953163.1953263
25. D. Kopta, J. Spjut, E. Brunvand, A. Davis, "Efficient MIMD Architectures for High-Performance Ray Tracing," International Conference on Computer Design (ICCD), Oct 2010. https://doi.org/10.1109/ICCD.2010.5647555
26. D Nellans, K. Sudan, E. Brunvand, R. Balasubramonian, "Improving Server Performance on Multi-Cores via Selective Off-loading of OS Functionality, International Conference on Computer Architecture (ISCA), Saint-Malo, France, June 2010. https://doi.org/10.1007/978-3-642-24322-6_23
27. D Nellans, K. Sudan, E. Brunvand, R. Balasubramonian, "Hardware Prediction of OS Run-Length for Fine-Grained Resource Customization, ISPASS, March 2010. https://doi.org/10.1109/ISPASS.2010.5452057
28. J. Spjut, A. Kensler, and E. Brunvand, "Hardware-Accelerated Gradient Noise for Graphics," ACM Great Lakes Conference on VLSI (GLSVLSI09), May 2009. https://doi.org/10.1145/1531542.1531647
29. D. Kopta, J. Spjut, E. Brunvand, and S. Parker, "Comparing Incoherent Ray Performance of TRaX vs. Manta," *IEEE Symposium on Interactive Ray Tracing*, August 2008. https://doi.org/10.1109/RT.2008.4634646
30. Peter Shirley, Kelvin Sung, Erik Brunvand, Alan Davis, Steven Parker, and Solomon Boulos. "Fast ray tracing and the potential effects on graphics and gaming courses." Comput. Graph. 32, 2 (April 2008). https://doi.org/10.1016/j.cag.2008.01.007
31. J. Spjut, D. Kopta, S. Boulos, S. Kellis, and E. Brunvand, "TRaX: A multi-threaded architecture for real-time ray tracing," In *6th IEEE Symposium on Application Specific Processors (SASP)*, June 2008 https://doi.org/10.1109/SASP.2008.4570794 ***Awarded Best Paper at SASP08***.
32. P. Shirley, K. Sung, E. Brunvand, A. Davis, S. Parker, S. Boulos, "Rethinking Graphics and Gaming Courses Because of Fast Ray Tracing", *SIGGRAPH Educator's Workshop*, 2007. https://doi.org/10.1145/1282040.1282056
33. Sven Woop, Erik Brunvand, and Philipp Slusallak, "Estimating Performance of an Ray Tracing ASIC Design," IEEE Symposium on Interactive Ray Tracing (RT06), September 2006. https://doi.org/10.1109/RT.2006.280209
34. Jung-Lin Yang and Erik Brunvand, "Improved Technique on Parallelism for Asynchronous Controllers," 17th VLSI Design / CAD Symposium, Taiwan, 2006.
35. Jung-Lin Yang, Erik Brunvand, and Sung-Min Lin, "HDL Modeling for Optimization and Verification of Asynchronous Controllers," International Symposium on Intelligent Signal Processing and Communication Systems, ISPACS 2005, Hong Kong, December 2005. https://doi.org/10.1109/ISPACS.2005.1595378
36. Jung-Lin Yang and Erik Brunvand, "Self-Timed Circuits Using DCVSL Semi-Bundled Delay Wrappers," International Symposium on Intelligent Signal Processing and Communication Systems, ISPACS 2005, Hong Kong, December 2005. https://doi.org/10.1109/ISPACS.2005.1595441
37. David Nellans, Rajeev Balasubramonian and Erik Brunvand, "A Case for Increased Operating System Support in Chip Multi-Processors," Second IBM Watson Conference on Interaction between Architecture, Circuits, and Compilers, PAC^2, New York, September 2005. http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.100.6331
38. Gaurav Gulati and Erik Brunvand, "Design of a Cell Library for Asynchronous Microengines," Great Lakes Symposium on VLSI, April 2005. https://doi.org/10.1145/1057661.1057753
39. Jung-Lin Yang and Erik Brunvand, "Pseudo Dynamic DCVSL Template For Power-Conservative Design," 16th VLSI Design / CAD Conference, Taiwan, 2005
40. Jung-Lin Yang, Erik Brunvand, and Sung-Min Lin, "HDL Modeling for Optimization and Verification Of Extended Burst-Mode Machines," 16th VLSI Design / CAD Conference, 2005. https://doi.org/10.1109/ISPACS.2005.1595378
41. Niti Madan and Erik Brunvand, "Asynchronous Microengines for Network Processing," International Conference on Information Systems: New Generations (ISNG 2004), Las Vegas, November 2004.

42. Niti Madan and Erik Brunvand, "A Case for Asynchronous Microengines for Network Processors," Advanced Networking and Communications Hardware Workshop (ANCHOR) 2004, Munich, Germany, (held in conjunction with ISCA) June 2004. http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.450.4089&rep=rep1&type=pdf
43. David Nellans, Vamshi Kadaru, and Erik Brunvand, "ARCsim: An Asynchronous Architectural Simulator," Great Lakes Symposium on VLSI (GLSVLSI), April 2004. https://doi.org/10.1145/988952.988970
44. Jung-Lin Yang and Erik Brunvand, "Using Dynamic Domino Circuits in Self-Timed Systems," Great Lakes Symposium on VLSI (GLSVLSI), April 2003. https://doi.org/10.1145/764808.764874
45. Jung-Lin Yang and Erik Brunvand, "Self-Timed Design with Dynamic Domino Circuits," IEEE Annual Symposium on VLSI Design, February 2003. https://doi.org/10.1109/ISVLSI.2003.1183473
46. Erik Brunvand and Chris Myers, Eds., "Advanced Research in VLSI," IEEE Press, April 2001. ISBN: 076951037X
47. Erik Brunvand and Chris Myers, Eds., "Asynchronous Circuits and Systems," IEEE Press, April 2001, ISBN: 0-7695-1034-5
48. Hans Jacobsen, Erik Brunvand, Ganesh Gopalakrishnan, and Prabhakar Kudva, "High Level Asynchronous System Design Using the ACK Framework," In International Conference on Advanced Research in Asynchronous Circuits and Systems (Async2000), Eilat, Israel, April 2000. https://doi.org/10.1109/ASYNC.2000.836975
49. Erik Brunvand, Steven Nowick, and Kenneth Yun, " Practical Advanced in Asynchronous Design and in Asynchronous/Synchronous Interfaces" Design Automation Conference, DAC-99, New Orleans, LA, June 1999. https://doi.org/10.1109/ICCD.1997.628936
50. Erik Brunvand, Steven Nowick, and Kenneth Yun, "Modern Asynchronous Circuit Design," TAU-99, Monterey, CA, March 1999. http://users.ece.cmu.edu/~chraska/tau99/
51. J. Carter, W. Hsieh, L. Stoller, M. Swanson, L. Zhang, E. Brunvand, A. Davis, C.-C. Kuo, R. Kuramkote, M. Parker, L. Schaelicke, and T. Tateyama, "Impulse: Building a Smarter Memory Controller," Symposium on High Performance Computer Architecture (HPCA), Jan 1999. https://doi.org/10.1109/HPCA.1999.744334
52. J. Carter, W. Hsieh, M. Swanson, L. Zhang, E. Brunvand, A. Davis, M. Parker, L. Schaelicke, L. Stoller, and T. Tateyama. "Memory System Support for Irregular Applications," Fourth Workshop on Languages, Compilers, and Run-time Systems for Scalable Computers (LCR '98), May 1998. https://doi.org/10.1007/3-540-49530-4_2
53. Erik Brunvand, Steven Nowick, and Kenneth Yun, "Practical Advances in Asynchronous Design," International Conference on Computer Design (ICCD 97). https://doi.org/10.1109/DAC.1999.781284
54. Ajay Khoche and Erik Brunvand, "Critical Hazard-Free Test Generation for Asynchronous Circuits," VLSI Test Symposium (VTS'97). https://doi.org/10.1109/VTEST.1997.600270
55. Ajay Khoche and Erik Brunvand, "ACT: A DFT Tool for Self-Timed Circuits," International Test Conference (ITC'97). https://doi.org/10.1109/TEST.1997.639697
56. William Richardson and Erik Brunvand, "Fred: A Decoupled Self-Timed Computer," In International Conference on Advanced Research in Asynchronous Circuits and Systems (Async96), Aizu, Japan, March 1996. https://doi.org/10.1109/ASYNC.1996.494438
57. Sandeep Pagey, Ajay Khoche and Erik Brunvand, "DFT for Fast Testing of Self-Timed Control Circuits," 4th IEEE Asian Test Symposium, 1995. https://doi.org/10.1109/ATS.1995.485364
58. William Richardson and Erik Brunvand, "Precise Exception Handling for a Self-Timed Processor," in IEEE International Conference on Computer Design (ICCD95). https://doi.org/10.1109/ICCD.1995.528787 ***Awarded best paper award at ICCD95***.
59. Ajay Khoche and Erik Brunvand, "Testing Self-Timed Circuits using Partial Scan," in 2nd Working Conference on Asynchronous Design Methodologies, South Bank University, London, May 1995. https://doi.org/10.1109/WCADM.1995.514653
60. Ajay Khoche and Erik Brunvand, "A Partial-Scan Methodology for Testing Self-Timed Circuits," in 13th IEEE VLSI Test Symposium, Princeton, NJ, April 1995. https://doi.org/10.1109/VTEST.1995.512650

61. John F. Hurdle, Erik L. Brunvand, and Lüli Josephson. "Asynchronous VLSI design for neural system implementation." International workshop on VLSI for neural networks and artificial intelligence, José G. Delgado-Frias and William R. Moore (Eds.). Plenum Press, New York, NY ISBN:0-306-44722-3
62. Erik Brunvand, "Low Latency Self-Timed Flow Through FIFOs," in 16th Conference on Advanced Research in VLSI, Chapel Hill, NC, March 1995. https://doi.org/10.1109/ARVLSI.1995.515612
63. Jae-Tack Yoo, Erik Brunvand, and Kent Smith, "Automatic Prototyping of Semi-Custom Integrated Circuits using Actel FPGAs," in Fifth Great Lakes Symposium on VLSI, Buffalo, NY, March 1995. https://doi.org/10.1109/GLSV.1995.516042
64. Ajay Khoche and Erik Brunvand, "Testing Micropipelines," In International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async94), November 1994. https://doi.org/10.1109/ASYNC.1994.656316
65. Ganesh Gopalakrishnan, Prabhakar Kudva, and Erik Brunvand, "Peephole Optimization of Asynchronous Macromodule Networks," In IEEE International Conference on Computer Design (ICCD), 1994. https://doi.org/10.1109/ICCD.1994.331946
66. Prabhakar Kudva, Ganesh Gopalakrishnan, and Erik Brunvand, "Performance Analysis and Optimization of Asynchronous Circuits," In IEEE International Conference on Computer Design (ICCD), 1994. https://doi.org/10.1109/92.748198
67. Joe Novak and Erik Brunvand, "Using FPGAs to Prototype a Self-Timed Floating Point Co-Processor," In IEEE Custom Integrated Circuits Conference (CICC), 1994. https://doi.org/10.1109/CICC.1994.379761
68. Lüli Josephson, Erik Brunvand, John F. Hurdle, and Ganesh Gopalakrishnan, "Reliable Interface Design for Combining Asynchronous and Synchronous Circuits," In Fifth NASA Symposium on VLSI Design, Albuquerque, New Mexico. November 1993. https://archive.org/stream/nasa_techdoc_19940016606/19940016606_djvu.txt
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71. Erik Brunvand, "Windchime: An FPGA-based Self-Timed Parallel Processor," In 3rd International Workshop on Field Programmable Logic and Applications, Oxford, September, 1993. ISBN:0-9518453-1-4
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73. Erik Brunvand, "The NSR Processor," In 26th Hawaiian International Conference on System Sciences, Maui, Hawaii, Jan 1993. https://doi.org/10.1109/HICSS.1993.270622
74. John F. Hurdle, Erik Brunvand, Lüli Josephson, and Ganesh Gopalakrishnan, "Asynchronous Models for Large Scale Neurocomputing Applications," In Fifth International Conference on Neural Networks and their Applications, Nimes, France, November 1992. https://doi.org/10.1007/978-1-4899-1331-9_13
75. Erik Brunvand, Nick Michell, and Kent Smith, "A Comparison of Self-Timed Design using FPGA, CMOS, and GaAs Technologies," In IEEE International Conference on Computer Design (ICCD), Cambridge, Mass., October 1992. https://doi.org/10.1109/ICCD.1992.276203
76. John F. Hurdle, Erik Brunvand, and Lüli Josephson, "Asynchronous VLSI Design for Neural System Implementation," In Third International Workshop on VLSI for Neural Networks and Artificial Intelligence, Oxford, September 1992.
77. Erik Brunvand, "Using FPGAs to Prototype a Self-Timed Computer," In 2nd International Workshop on Field-Programmable Logic and Applications, Vienna Institute of Technology, August 1992.
78. Erik Brunvand, "Implementing Self-Timed Systems with FPGAs," In International Workshop on Field Programmable Logic and Applications, Oxford, September, 1991.

79. Erik Brunvand and Mike Starkey, "An Integrated Environment for the Design and Simulation of Self-Timed Systems," In *VLSI-91*, IFIP, August 1991. https://dblp.org/db/conf/vlsi/vlsi1991
80. Erik Brunvand and Robert F. Sproull, "Translating Concurrent Programs into Delay-Insensitive Circuits," In IEEE International Conference on Computer-Aided Design *ICCAD-89*, November 1989. https://doi.org/10.1109/ICCAD.1989.76949

Publications — Refereed Conference talks, panels, posters, etc. — Student authors are underlined.....

1. S. Reiser, E. Brunvand, P. Conrad, C. Starrett, W. Kirby, " CS+Art Curriculum," ACM SIGCSE (panel), Baltimore, MD, Feb 2018. https://doi.org/10.1145/3159450.3159466
2. S. Reiser, E. Brunvand, P. Conrad, C. Starrett, C. Reas, "Curriculum Matters: Melding Art + Computer Science," ACM SIGGRAPH (panel), Los Angeles, CA, August 2017. http://s2017.siggraph.org/educators-forum.html
3. Erik Brunvand, "CS+X: Cross Campus Collaborations," ACM SIGGRAPH 2016 (panel), Anaheim, CA, August 2016. http://s2016.siggraph.org/educators-forum.html
4. E. Brunvand, "Kinetic Sculptures: Creating Programmable Art," ACM SIGGRAPH 2015 (studio course), Los Angles, CA, August 2015. http://s2015.siggraph.org/attendees/studio-courses.html
5. E. Brunvand and S. Brunvand, "Drawing Machines: An Arts and Engineering Collaboration," NAEA conference, San Diego, CA, Mar 2014. http://naeaworkspace.org/naea14_handouts/
6. E. Brunvand, "Automated Drawing: Exploring the Boundaries between Print and Drawing," Impact8, Dundee, Scotland, August 2013. ISBN: 1 899837 70 1. http://www.conf.dundee.ac.uk/impact8/publication/
7. E. Brunvand, "Electrified Printmaking: Using Conductive Ink to Create Active Images," Impact8, Dundee, Scotland, August 2013. ISBN: 1 899837 70 1. http://www.conf.dundee.ac.uk/impact8/publication/
8. Erik Brunvand, "Automated Drawing Machines: Blurring the Line between Drawing and Print," Southern Graphics Council International (SGCI) conference, Minneapolis, MN, Mar 2013. http://jessicameuninck.com/uwm/wp-content/uploads/2016/01/ConferenceProgram3_6_13.pdf
9. Konstantin Shkurko, Thiago Ize, Christiaan Gribble, Erik Brunvand, and Lee Butler, "Simulating Radio Frequency Propagation via Ray Tracing," GPU Technology Conference, March 2013 (poster).
10. Erik Brunvand, Paul Stout, "Collaborative Design Experience with Kinetic Sculpture." College Art Association Conference (CAA), Los Angeles, CA, Feb 2012. https://www.collegeart.org/programs/conference
11. Erik Brunvand, Al Denyer, "Printmaking on a Micro Scale: An Art and Science Collaboration ," Southeastern College Art Conference (SECAC), Savannah, GA, Nov 2011. https://secacart.org/page/ConferenceHistory
12. E. Brunvand, A. Denyer "Printmaking at a Micro Scale," Impact Multidisciplinary Printmaking Conference, Bristol, U.K., September 2009. https://www.uwe.ac.uk/sca/research/cfpr/dissemination/conferences/impact.html
13. D. Kopta, J. Spjut, and E. Brunvand, "Grid-based Ray Tracing with CUDA," (poster) ACM/Eurographics High Performance Graphics, New Orleans, August 2009. https://dl.acm.org/citation.cfm?id=1572769
14. E Brunvand, "Printmaking with Extreme Technology, Southern Graphics Council Conference, Chicago, March 2009. https://www.sgcinternational.org/conference/past-conferences/
15. Erik Brunvand, "Bugs and Glitches in Computer Folklore", American Folklore Society, Austin TX, October 1997.
16. Erik Brunvand, "The Heroic Hacker: Legends of the Computer Age," American Folklore Society, Pittsburgh PA, October 1996.

Publications — Technical Reports — Student authors are underlined.

1. Konstantin Shkurko, Tim Grant, Erik Brunvand, Daniel Kopta, Josef Spjut, Elena Vasiou, Ian Mallett, and Cem Yuksel, "SimTRaX: Simulation Infrastructure for Exploring Thousands of Cores," University of Utah, School of Computing, UUCS-18-001, 2018.
2. Daniel Kopta, Andrew Kensler, Thiago Ize, Josef Spjut, Erik Brunvand, Al Davis, "Fast, Effective BVH Updates for Dynamic Ray-Traced Scenes Using Tree Rotations," University of Utah, School of Computing, UUCS-11-002, 2011.
3. David Nellans, Rajeev Balasubramonian, and Erik Brunvand, "Interference Aware Cache Designs for Operating System Execution," University of Utah, School of Computing, UUCS-09-002, 2009.
4. Sven Woop, Erik Brunvand, and Philipp Slusallek, "HWML: RTL/Structural Hardware Description using ML," Technical Report, Computer Graphics Lab, Saarland University, 2006.
5. Gaurav Gulati and Erik Brunvand, "A Cell Library for Asynchronous Microengines," Technical Report, University of Utah, School of Computing, Jan 2005.
6. Franklin Prosser, David Winkel, and Erik Brunvand, "A comparison of modular self-timed design styles," University of Utah, Department of Computer Science, UUCS-95-025.
7. William F. Richardson and Erik Brunvand, "Fred: An Architecture for a Self-Timed Decoupled Computer," Technical Report UUCS-95-008, University of Utah, Department of Computer Science, 1995.
8. Ajay Khoche and Erik Brunvand, "A Partial Scan Methodology for Testing Self-Timed Circuits," Technical Report UUCS-95-001, University of Utah, Department of Computer Science, 1995.
9. Erik Brunvand, "Reduced Latency Self-Timed FIFO Circuits," Technical Report UUCS-94-037, University of Utah, Department of Computer Science, 1994.
10. Jae-Tack Yoo, Erik Brunvand, and Kent Smith, "Automatic Rapid Prototyping of Semi-Custom VLSI Circuits using FPGA's," Technical report UUCS-94-022, University of Utah, Department of Computer Science, 1994.
11. Prabhakar Kudva, Ganesh Gopalakrishnan, and Erik Brunvand, "Performance Analysis and Optimization of Asynchronous Circuits," Technical Report UUCS-94-015, University of Utah, 1994.
12. Nick Michell, Erik Brunvand, and Kent Smith, "A Gallium Arsenide Mutual Exclusion Element," Technical Report UUCS-93-029, University of Utah, Department of Computer Science, 1993.
13. Erik Brunvand and Nick Michell, "Speed without Fear: Composable Self-Timed GaAs Circuits," Technical Report UUCS-93-028, University of Utah, Department of Computer Science, 1993.
14. Ganesh Gopalakrishnan, Erik Brunvand, and Nick Michell, "A Correctness Criterion for Asynchronous Circuit Validation and Optimization," Technical Report UUCS-92-004, University of Utah, 1992.
15. William Richardson and Erik Brunvand, "The NSR Processor Prototype," Technical Report UUCS-92-029, University of Utah, Department of Computer Science, 1992.
16. Erik Brunvand, "A Cell Set for Self-Timed Design using Actel FPGAs," Technical Report UUCS-91-013, University of Utah, Department of Computer Science, 1991.
17. Erik Brunvand and Robert F. Sproull, "Translating Concurrent Communicating Programs into Delay Insensitive Circuits," Technical Report CMU-CS-89-126, Carnegie Mellon University, 1989.
18. Erik Brunvand, "Parts-R-Us: A Chip Aparts," Technical Report CMU-CS-87-119, Carnegie Mellon University, 1987.
19. Erik Brunvand and Ivan E. Sutherland, "An Asynchronous Q-Bus Interface," Technical Memo 4677, Sutherland, Sproull, and Associates, 1986.

Publications — Dissertation and Thesis

1. Erik Brunvand, "Translating Concurrent Communicating Programs into Asynchronous Circuits," Ph.D. Dissertation, Carnegie Mellon University, 1991 (Available as Technical Report CMU-CS-91-198). pages)
2. Erik Brunvand, "Context Addressable Memory for Symbolic Processing Systems," Masters Thesis, University of Utah, 1984.

Patents

1. Erik Brunvand and Alan Davis, "Circulating Context Addressable Memory," U.S. Patent No. 4,924,435, issued May 8 1990.
2. Erik Brunvand, Alan Davis, and Ian Robinson, "Memory Apparatus and Method for Retrieving Sequences of Symbols Including Variable Elements," U.S. Patent No. 4,748,439, issued May 31, 1988.

Software

1. K. Shkurko, T. Grant, E. Brunvand, D. Kopta, J. Spjut, E. Vasiou, I. Mallett, C. Yuksel, "SimTRaX: Simulation Infrastructure for Exploring Thousands of Cores, `https://code.google.com/archive/p/simtrax/` `http://utaharch.blogspot.com/2012/06/introducing-simtrax.html`

INVITED TALKS

- Since 2015 I have been a member of the *ACM Distinguished Speaker Program* - an ACM program to identify excellent speakers that are supported by ACM when requested to speak at various events and conferences. `https://speakers.acm.org/speakers/brunvand_6382`

Keynote Addresses

- "NSF Funding Priorities and Opportunities," Workshop on the Future of FPGA Acceleration in Cloud and Data Centers (FCCM 2020), Virtual Event, May 2020.
- "Computational Thinking Meets Design Thinking: Technology and Arts Collaborations," VLSI Design / CAD Conference, Kolkata, India, January 2016. (*ACM Distinguished Speakers Program talk*)
- "Computational Thinking Meets Design Thinking: Technology and Arts Collaborations," ACM Great Lakes Symposium on VLSI, Pittsburgh, PA, May 2015. (*ACM Distinguished Speakers Program talk*)
- "Twenty Years of Async," IEEE Symposium on Asynchronous Circuits and Systems, Potsdam, Germany, May 2014.
- "The Heroic Hacker: Computer Folklore and Hacker Culture," IEEE Symposium on Asynchronous Circuits and Systems, Santa Monica, CA, May 2013.
- "High Performance Ray Tracing: Implications for System Architectures," IEEE/IFIP VLSI-SoC conference, Oct 2012.
- "The State of Self-Timed Circuit Design," 2nd Working Conference on Asynchronous Design Methodologies, South Bank University, London, May 1995.

Invited Talks & Workshops & Conference Special Sessions

- "Arts and Technology Collaborations," Iowa State University, HCI Graduate Program, Ames Iowa, April 2023 (*ACM Distinguished Speakers Program talk*)
- Organized "Educator's Forum" paper session at ACM SIGGRAPH 2019, Los Angeles, CA (papers from ACM SIGCSE 2019 re-presented at SIGGRAPH 2019).
- "Arts and Technology Collaborations," College of Charleston, Charleston, S.C. , April 2019 (*ACM Distinguished Speakers Program talk*)
- Organized "Sister SIG" paper session at ACM SICGCE 2019, Minneapolis, MN (papers from ACM SIGGRAPH 2018, re-presented at SIGCSE 2019).
- Organized "Educator's Forum" paper session at ACM SIGGRAPH 2018, Vancouver, BC (papers from ACM SIGCSE 2018 re-presented at SIGGRAPH 2018).
- Organized "Sister SIG" paper session at ACM SICGCE 2018, Seattle, WA (papers from ACM SIGGRAPH 2017, re-presented at SIGCSE 2018).
- "Drawing Machines : Mechanical Computer Graphics," Workshop at University of Redlands, Redlands, CA, January, 2018.
- Circuit Bending Workshop, Music Department, Harvard University, March 2018.

- Organized “Educator’s Forum” paper session at ACM SIGGRAPH 2017, Los Angeles, CA (papers from ACM SIGCSE 2017 re-presented at ACM SIGGRAPH 2017).
- “A Tale of Two Rendering Algorithms: Ray Tracing, Rasterization, and their Supporting Hardware," University of Richmond, Richmond, VA, January 2017.
- “Hardware Support for High Performance Ray Tracing,” Indian Statistical Institute, Kolkata, India, January 2016.
- “Arts and Technology Collaborations,” University of Calcutta, Kolkata, India, January, 2016
- “Hardware Support for High Performance Ray Tracing,” Indian Institute of Technology (IIT), Delhi, December 2015.
- “Drawing Machines: An Arts and Engineering Collaboration,” Visiting artist lecture, Frostic School of the Arts, Western Michigan University, Kalamazoo, MI, April 2015.
- “Drawing Machines: Mechanical Computer Graphics,” Workshop at Frostic School of the Arts, Western Michigan University, Kalamazoo, MI, November 2015.
- “Circuit Bending: The Science of Breaking Toys,” TEDx Salt Lake City, Sept 2015. `https://www.tedxsaltlakecity.com/event-archive/2015`
- “Computer Controlled Drawing Machines,” Workshop at the International Sculpture Conference: New Frontiers in Sculpture, Phoenix, AZ, April 2015. `https://www.sculpture.org/az2015/activities.shtml`
- “Drawing Machines: Mechanical Computer Graphics,” Studio workshop and contest, SIGGRAPH, Vancouver, Canada, 2014
- “Drawing Machines and Arts Tech Collaborations,” Snow College visiting artists lecture series, Ephraim, UT, April, 2014
- “Design Thinking meets Computational Thinking: Kinetic Art and Embedded Systems,” Newcastle University, Newcastle, U.K., August 2013
- “Arts and Technology: Strange Bedfellows or Congenial Colleagues?," Western State Colorado University, Gunnison, Colorado, April, 2013
- “Embedded Systems and Kinetic Art,” University of Washington, Seattle, Nov 2012.
- “Embedded Systems and Kinetic Art,” Microsoft Research Labs, Redmond, WA, Oct 2012.
- “Arts and Technology: Strange Bedfellows or Congenial Colleagues?," College of Charleston, Charleston, S.C., Nov 2011.
- “Hardware Support for Interactive Ray Tracing,” Columbia University, New York, February 2006.
- “Asynchronous and Self-Timed System Design,” University of Saarland, October 2005.
- “A New Course in Arithmetic Circuits,” David Evans Conference on Computer Engineering, Midway, Utah, June 2005
- “A Computer Engineering Grad Curriculum” David Evans Conference on Computer Engineering, Midway, Utah, June 2004.
- “Teaching VLSI: CAD Tools, Chips and Challenges,” David Evans Conference on Computer Engineering, Midway, Utah June 2003.
- “Fred, an Asynchronous Microprocessor,” CS Department, South Bank University, London, England, May 1999.
- “Asynchronous Processor Design,” Computer Science Department, South Bank University, London, England, April 1999.
- “Fred, an Asynchronous Microprocessor,” Computer Science Department, University of Manchester, Manchester, England, April 1999.
- “Asynchronous Processor Design,” Computer Science Department, University of Manchester, Manchester, England, March 1999.
- “Modern Asynchronous Circuit Design,” Computer Science Department, University of Washington, Seattle, November 1998.
- “The Avalanche Multiprocessor,” Computer Science Department, Carnegie Mellon University, October 1996.
- “Self-Timed Circuits and FIFOs,” Electrical Engineering Department, Cornell University, October 1995.
- “Self-Timed Circuits and FPGAs,” Computer Science Department, University of Waterloo, Waterloo, Canada, April 1994.
- “Windchime: A Self-Timed Parallel Computer,” Computer Science Department, Technical University of Denmark, Lyngby, Denmark, September 1993.

- "The NSR Processor Architecture," Computer Science Department, University of Manchester, Manchester, England, August 1993.
- "The NSR Processor Architecture," Sun Microsystems Laboratories, Mountain View, CA, November 1992.
- "The NSR Processor FPGA Prototype," Actel Corporation, Sunnyvale, CA, November 1992.
- "Implementing Self-Timed Circuits with FPGAs," DEC Paris Research Labs, Paris, France, August 1992.
- "The NSR Processor," Computer Science Department, Stanford University, Stanford, CA, July 1992.
- "The NSR Processor FPGA Prototype," National Science Foundation, workshop on Integrating FPGAs Into Microelectronics Education, Washington, D.C., July 1992.
- "Translating Concurrent Programs into Asynchronous Circuits," Computer Science Department, University of Washington, Seattle, WA, September 1989.
- "Translating occam programs into Self-Timed Circuits," HP Labs, Palo Alto, CA, August 1989.
- "Translating occam programs into Self-Timed Circuits," Apple Computer, Advanced Technology Group, Cupertino, CA, August 1989.

Major Media Exposure

- KSL News, Making Noise about Technological Fluency, Peter Rosen reporting, May 25, 2016: `https://www.ksl.com/article/39904916/making-noise-about-technologicalfluency`
- TEDx Talk: "Circuit Bending: The Science of Breaking Toys," TEDx Salt Lake City, Sept 2015. `https://www.tedxsaltlakecity.com/event-archive/2015`

GRANTS & CONTRACTS

= Research, = Education, = Conference Support

Hardware Ray Tracing **2023-2026**
Meta Corp. *$841,307 (my share = $420,653)*
My role: co-PI (Cem Yuksel PI)

Curricular Design for Broadening Participation through Computing in the Arts **2019-2023**
National Science Foundation *$325,000 ($70,000 Utah share)*
My role: co-PI (Erin Parker PI)

John R. Park Teacher's Fellowship **2019**
Teaching Committee, University of Utah *$10,000*
My role: PI

Architectures for Energy Efficient Ray Tracing **2014–2019**
National Science Foundation *$899,992*
My role: PI (Cem Yuksel Co-PI)

Intel/Altera Educational Donation (Gift of Altera prototyping boards) **2018**
Intel Inc. *Equipment worth $10,800*
My role: PI (Matching gift for BEEF funds)

IEEE Symposium on Asynchronous Circuits and Systems **2017**
Oracle, Inc. *$6000*
My role: PI

Makerspace Equipment: 3D Printers **2017**
BEEF funds *$18,000*
My role: PI

IEEE Symposium on Asynchronous Circuits and Systems **2016**
Oracle, Inc. *$6000*
My role: PI

Makerspace Equipment: Laser Cutter **2016**
BEEF funds *$24,457*
My role: PI

IEEE Symposium on Asynchronous Circuits and Systems **2015**
Oracle, Inc. *$6000*
My role: PI

Flexible Architectures for Future Graphics Processing Systems **2010–2014**
National Science Foundation *$499,709*
My role: PI (Al Davis, Co-PI)

University Professorship **2014–2016**
Undergraduate Studies, University of Utah *$35,000*
My role: PI

University Teaching Assistantship **2014–2015**
Graduate School, University of Utah *$15,000*
My role: PI

IEEE Symposium on Asynchronous Circuits and Systems **2014**
Oracle, Inc. *$3000*
My role: PI

IEEE Symposium on Asynchronous Circuits and Systems **2013**
Oracle, Inc. *$3000*
My role: PI

Radio Frequency Ray Tracing **2012–2013**
Army Research Labs (ARL) *$85,000*
My role: PI

The Big Draw: Art and Engineering Collaboration in Automated Drawing **2011–2012**
Council of Dee Fellows, University of Utah *$8,400*
My role: PI (Paul Stout Co-PI)

Radio Frequency Ray Tracing Evaluation **2011**
Army Research Labs (ARL) *$37,384*
My role: PI

IEEE Symposium on Asynchronous Circuits and Systems **2011**
Oracle, Inc. *$3000*
My role: PI

Hardware Support for Real Time Ray Tracing — **2006–2010**
National Science Foundation — *$505,382*
My role: PI (Al Davis, Co-PI)

University Teaching Assistantship — **2010–2011**
Graduate School, University of Utah — *$15,000*
My role: PI

Embedded Systems and Kinetic Art — **2009**
Teaching Committee, University of Utah — *$4,300*
My role: PI (Paul Stout Co-PI)

IODrive 160GB solid state memory card — **2009**
Fusion IO, Inc. — *Equipment worth $6,570*
My role: PI (David Nellans Co-PI)

Xilinx Educational Donation (Gift of Xilinx prototyping boards) — **2009**
Xilinx, Inc. — *Equipment worth $4,200*
My role: PI — (Matching gift for BEEF funds)

Ray Trace Applications to Radio Frequency(RF) Propogation — **2007–2008**
Army Research Labs (ARL) — *$140,087*
My role: PI

Engineering/Art Collaborative Course — **2007**
Teaching Committee, University of Utah — *$7,075*
My role: PI (Justin Diggle, Co-PI)

High-Performance Asynchronous Computer Architecture — **2002–2006**
National Science Foundation — *$325,000*
My role: PI

Xilinx Educational Donation (Gift of Xilinx prototyping boards) — **2006**
Xilinx, Inc. — *Equipment worth $2,493*
My role: PI

Cadence Design Flow Support — **2005**
Cadence, Inc. — *$2,000*
My role: PI

John R. Park Teacher's Fellowship — **2005**
Teaching Committee, University of Utah — *$10,000*
My role: PI

University Teaching Assistantship — **2004–2005**
Graduate School, University of Utah — *$11,000*
My role: PI

Microengines for Programmable Self-Timed Control — **2000-2004**
National Science Foundation — *$412,914*
My role: PI (Ganesh Golapalakrishnan Co-PI)

Support for the IEEE ASYNC 2001 Symposium at the University of Utah **2001**
Sun Microsystems Inc. *$20,000*
My role: PI

Support for the IEEE ASYNC 2001 Symposium at the University of Utah **2001**
Intel Inc. *$2,000*
My role: PI

Support for ARVLSI 2001 Conference at the University of Utah **2001**
Intel Inc. *$1,500*
My role: PI

Computer Engineering Lab Enhancement **2001**
Governor's Initiative in Engineering *$110,000*
My role: PI

Impulse: Adaptive Memory Systems **1998–2001**
ARPA, Adaptive Computer Systems *$2,700,000*
My role: Co-PI (John Carter, PI, Mark Swanson Co-PI)

Center of Excellence in Asynchronous Circuit and System Design **1997–2000**
Utah State Centers of Excellence Program *$300,000*
My role: PI (Chris Myers, also PI)

Application-Driven Advancement of Asynchronous Design Methods **1996–2000**
National Science Foundation *$503,291*
My role: PI (Ganesh Gopalakrishnan Co-PI

Communication and Memory Architectures for Scalable Parallel Computing (Avalanche) **1995–1998**
ARPA/SPAWAR *$4,700,000*
My role: Co-PI (Al Davis PI, John Carter and Mark Swanson Co-PIs)

Advanced Research in Asynchronous Circuits and Systems **1994–1995**
National Science Foundation *$12,300*
My role: PI (Ganesh Gopalakrishnan, Steve Nowick Co-PIs)

The Design of Asynchronous Circuits and Systems **1993–1996**
National Science Foundation *$240,000*
My role: PI (Ganesh Gopalakrishnan Co-PI

Testing Asynchronous Circuits **1993–1995**
University of Utah Research Committee *$5,000*
My role: PI

Self-Timed GaAs Building Blocks for High Performance Systems **1992–1994**
National Science Foundation *$110,000*
My role: Co-PI (Kent Smith, PI)

Asynchronous Computer Architecture **1991–1994**
National Science Foundation *$70,000 + $10,000 UofU matching funds*
My role: PI

Building Blocks for Implementing Self Timed VLSI Circuits **1991–1993**
University of Utah Research Committee *$5,000*
My role: PI

Using FPGAs in the Classroom **1990**
National Science Foundation *$6,000*
My role: PI

TEACHING

Teaching Awards

- Awarded two-year University Professorship from the Undergraduate College at the University of Utah for the academic years 2014-2015 and 2015-2016. *"Every two years, at least one faculty member is selected for the special rank of University Professor. This professorship recognizes individuals who have demonstrated extraordinary skills in teaching, distinguished scholarship in their field, and an interdisciplinary approach to undergraduate instruction."*
- Awarded School of Computing Outstanding Teaching Award, 2012.
- Awarded University of Utah Distinguished Teaching Award for 2002-2003 (also nominated in 2001-2002).
- IEEE Nominee for Utah Engineers Council, Engineering Educator of the Year award, 2003.
- Awarded College of Engineering Outstanding Teaching Award for 1997.
- Awarded 31 Dean's Teaching Commendation Letters for outstanding student course evaluations since 1990. These letters go to professors in the top 15% of the college based on teaching evaluation scores.

STUDENT ADVISING

Chair of PhD Committee: Graduated Students

- Elena Vasiou, 2020, "Hardware for Ray-Conscious Ray Tracing"
- Konstantin Shkurko, 2018, "Dual Streaming for Hardware-Accelerated Ray Tracing"
- Daniel Kopta, 2015, "Ray Tracing from a Data Movement Perspective"
- David Nellans, 2014, "Improving Operating System and Hardware Interaction"
- Josef Spjut, 2013, "Hardware Support for Real Time Ray Tracing"
- Jung-Lin Yang, 2003, "Transistor Level Technology Mapping for Extended Burst-Mode Asynchronous Designs," (ECE Department)
- Lüli Josephson, M.Phil., 2001
- Ajay Khoche, 1996, "Testing Asynchronous Circuits"
- Bill Richardson, 1996, "Architectural Considerations in a Self-Timed Processor Design,"
- John Hurdle, 1994, "Smart Parts: Toward the Automated Synthesis of Neural Circuits,"

Chair of Masters Thesis Committee: Graduated Students

- Eli Ribble, 2009, "Visualizing 802.11 Wireless Connection Strength,"
- Ryan Romney, 2008, "Circuits for Computing Inverse Square Root" (ECE Departmnent)
- Gaurav Gulati, 2006, "A Cell Set and Library for Asynchronous Microengine Design" (ECE Department)
- Niti Madan, 2004, "Asynchronous Microengines for Network Processing"
- Himanshu Singh, 2004, "Asynchronous Microengines for DSP Applications" (ECE Department)
- Sudeesh Madayi, 2003, "A Self Timed Cell Set and Library" (ECE Department).
- Vamshi Krishna Kadaru, 2003, "Evaluation of Self Timed Library Circuits" (ECE Department).
- Mike Snider, 2003, "A CAD Tool for Self-Timed Design" (ECE Department).
- Harishankar Sridharan, 2002, "Evaluation of a Self-Timed Multiplier" (EE Department).
- David LeBaron,1997, "Self-Timed Arithmetic Circuits" (EE Department)
- Joe Novak, 1994, "A Self-Timed IEEE Floating Point Unit"
- Tom Wolf, 1992, "The A3000: A Self-Timed Version of the R3000"

Member of PhD Committee

Ian Mallett (2021), Mac Wibbles (2020), Meysam Taassori (2019), Ethan Kerzner (2018), Joe Novak (2018), Dipanjan Bhadra (2018), Ali Shafiee (2017), William Lee (2015), Tannu Sharma (2015), Manjunath Shevgoor (2015), Bennion Redd (2015), Andrzej Fory (2014), Seth Pugsley (2014), Christopher Condrat (2013), Vikas Vij (2013), Mike Parker

(2013), Shafagh Abbasi (2013), Bryan Willis (2012), Karthik Ramani (2012), Kshitij Sudan (2012), Roni Choudhury (2012), Aniruddha Udipi (2012), Eliyah Kilada (2012), Manu Awasthi (2011), Niti Madan (2009), Naveen Muralimanohar (2008), Liqun Cheng (2007), Sven Woop (External examiner for Sven at University of Saarland, 2007), Peter Jensen (2006), Hans Jacobson (2003), Eric Mercer (2002), Eric Peskin (2002), Hao Zheng (2001), Lambert Schaelicke (2001), Binu Mathew (2001), Ravi Kuramkote (2001), Wendy Belluomini (1999), Ravi Hosabetta (1999), Nick Michell (1997), Greg Hannon (1996), Kelly Jones, (1995), Prabhakar Kudva (1995)

Member of Masters Thesis Committee

Daqi Lin (2019), Mason Montazer (2017), Dheeraj Singh Takur (2016), Yang Shen (2016), …*gap in my record keeping* …, Anand Gopalan (2002), Chris Krieger (2001), Eric Mercer (1999), Brandon Bachman (1998), Robert Thacker (998), Hao Zhang (1998), Richard G. Burford (1995), Anthony Dobaj (1995), Kyle Johns (1994), V. Chandramouli (1993), Madhu Penugonda (1993), Prabhat Jain (1992), Prabhakar Kudva (1992)

Detailed Teaching Data

- Instructors with student evaluations in the top 15% of the College of Engineering receive a commendation letter from the Dean for their teaching accomplishments. 🎓
- The ratings for Effective Instructor and Effective Course are summary ratings from the student evaluation questions related to those areas. The S. Avg is the average for the School of Computing in that same semester. Ratings are on a scale from 1–6.

Semester	Course	Enrolled (Resp.)	Eff. Instr. (S. Avg)	Eff. Course (S. Avg)	Top 15%
S24	CS 5789 Embedded Sys and Kinetic Art	26			
F23	CS/ECE 4710 Comp Eng Capstone Project	22 (5)	5.80 ()	6.00 ()	
S23	CS/ECE 3992 Comp Eng Capstone Project Planning	23 (6)	5.17 (5.12)	5.83 (5.18)	
F22	CS/ECE 3710 Computer Design	35 (5)	5.80 (5.15)	5.60 (5.08)	
S22 … …F19	*On-leave during this period at the NSF as a Program Manager in CISE/CNS*				
S19	CS5789/ART4455 Embedded Systems & Kinetic Art	21 (5)	5.25 (5.32)	4.25 (5.20)	
S19	CS/ECE 3992 Comp Eng Capstone Project Planning	34 (15)	5.64 (5.32)	5.11(5.20)	
F18	CS/ECE 4710 Comp Eng Capstone Project	38 (8)	5.22 (5.40)	5.21(5.26)	
F18	ECE 4991 Computer Engineering Sr. Thesis	2			
S18	CS 2050 Sound Art and Digital Media	19 (7)	5.80 (5.33)	5.58 (5.25)	🎓
S18	CS/ECE 3992 Comp Eng Sr. Project Planning	44 (18)	5.46 (5.33)	5.04 (5.25)	
F17	CS/ECE 3991 Computer Engineering Jr. Seminar	56 (23)	5.52 (5.38)	5.20 (5.25)	
F17	CS/ECE 5710 Digital VLSI	24	*included with 6710 results*		
F17	CS/ECE 6710 Digital VLSI	16 (13)	4.07 (5.38)	3.77 (5.25)	
S17	CS/ECE 3700 Digital System Design	92 (52)	5.38 (5.20)	5.17 (5.17)	
S17	CS5789/ART4455 Embedded Systems & Kinetic Art	22 (10)	5.68 (5.20)	5.31 (5.17)	
F16	CS/ECE 3991 Computer Engineering Jr. Seminar	31 (11)	5.69 (5.37)	5.43 (5.19)	🎓
F16	CS/ECE 4710 Comp Eng Sr. Project	23 (4)	5.67 (5.37)	5.75 (5.19)	🎓
S16	CS/ECE 3992 Comp Eng Sr. Project Planning	18 (11)	5.72 (5.22)	5.56 (5.10)	🎓
S16	UGS/CS2050 Sound Art and Digital Media	24(12)	5.64 (5.22)	5.39 (5.10)	🎓
S16	CS6712 Digital VLSI Testing	9 (7)	5.61 (5.22)	5.63 (5.17)	🎓
F15	CS/ECE 5710 Digital VLSI	16	*included with 6710 results*		🎓
F15	CS/ECE 6710 Digital VLSI	60 (44)	5.75 (5.16)	5.58 (5.01)	🎓
F15	CS/ECE 3991 Computer Engineering Jr. Seminar	27 (11)	5.49 (5.16)	5.22 (5.01)	
S15	CS5789/ART4455 Embedded Systems & Kinetic Art	11 (9)	5.56 (5.22)	5.27 (5.10)	
S15	UGS2050 Sound Art and Digital Media	20 (9)	5.02 (5.18)	5.11 (5.07)	
F14	CS/ECE 4710 Comp Eng Sr. Project	18 (10)	5.72 (5.36)	5.61 (5.21)	🎓
S14	CS/ECE 3992 Comp Eng Sr. Project Planning	23 (13)	5.64 (5.09)	5.63 (5.05)	🎓
S14	CS5789/ART4455 Embedded Systems & Kinetic Art	23 (13)	5.70 (5.09)	5.29 (5.05)	
S14	CS6712 Digital VLSI Testing	9 (5)	5.57 (5.09)	5.71 (5.05)	
F13	CS/ECE 5710 Digital VLSI	17 (11)	5.82 (5.29)	5.84 (5.13)	🎓
F13	CS/ECE 6710 Digital VLSI	35 (26)	5.52 (5.29)	5.38 (5.13)	
S13	*Sabbatical Leave*				
F12	*Sabbatical Leave*				
S12	CS/ECE 3700 Digital System Design	92 (51)	5.36 (5.36)	5.29 (5.19)	
S12	CS5789/ART3490 Embedded Systems & Kinetic Art	23 (16)	5.48 (5.36)	4.88 (5.19)	
S12	CS6712 Digital VLSI Testing	6 (2)	6.0 (5.36)	6.0 (5.19)	
F11	CS/ECE 5710 Digital VLSI	13	*included with 6710 results*		🎓
F11	CS/ECE 6710 Digital VLSI	33 (17)	5.59 (5.24)	5.60 (5.08)	🎓
F11	CS/ECE 3991 Computer Engineering Jr. Seminar	21 (13)	5.64 (5.24)	5.35 (5.08)	🎓
F11	CS6965 Parallel HW Ray Tracing	8 (2)	5.71 (5.24)	6.0 (5.08)	

Semester	Course	Enrolled (Resp.)	Eff. Instr. (S. Avg)	Eff. Course (S. Avg)	Top 15%
S11	CS/ECE 5830 VLSI Architecture	5	*included with 6830 results*		
S11	CS/ECE 6830 VLSI Architecture	21 (15)	5.39 (4.91)	5.35 (4.78)	
F10	CS/ECE 3710 Computer Design Lab	20 (16)	5.81 (5.17)	5.71 (5.07)	🎓
F10	CS5789/ART4455 Embedded Systems & Kinetic Art	20	*No numerical results on-line*		
F10	CS/ECE 3991 Computer Engineering Jr. Seminar	21 (19)	5.73 (5.17)	5.51 (5.07)	
S10	CS/ECE 3700 Digital System Design	90 (46)	5.84 (5.26)	5.56 (5.25)	🎓
S10	CS6712 Digital VLSI Testing	13 (6)	4.57 (5.16)	4.51 (4.96)	
F09	CS/ECE 5710 Digital VLSI	13 (8)	5.81 (5.34)	5.2 (5.18)	🎓
F09	CS/ECE 6710 Digital VLSI	31 (23)	5.91 (5.16)	5.80 (5.17)	🎓
F09	CS5968/FA3800 Sp.Topics: Emb. Sys. & Kinetic Art	9 (5)	5.74 (5.16)	5.60 (5.17)	🎓
F09	CS/ECE 3991 Computer Engineering Jr. Seminar	14 (5)	5.63 (5.34)	4.89 (5.18)	
F09	CS7940 HWRT Seminar	2			
S09	CS/ECE 5830 VLSI Architecture	29 (5)	5.91 (5.14)	5.60 (5.01)	🎓
S09	CS/ECE 6830 VLSI Architecture	9 (6)	5.39 (5.14)	5.10 (5.01)	
F08	CS/ECE 3710 Computer Design Lab	38 (12)	5.84 (5.20)	5.65 (5.18)	🎓
F08	CS7940 HWRT Seminar	2			
S08	CS/ECE 3700 Digital System Design	118 (45)	5.58 (5.13)	5.34 (5.00)	
S08	CS6712 Digital VLSI Testing	12 (7)	5.43 (5.13)	5.39 (5.00)	
F07	CS/ECE 5710 Digital VLSI	20 (10)	5.71 (5.21)	5.71 (5.12)	🎓
F07	CS/ECE 6710 Digital VLSI	30 (17)	5.50 (5.21)	5.47 (5.12)	🎓
F07	CS5965/Art6965 Special Topics: VLSI and Art	5	*No numerical results on-line*		
F07	CS7940 HWRT Seminar	4			
Student evaluation numerical summaries are available on-line only through Fall 2007					
S07	CS/ECE 6830 VLSI Architecture	12			🎓
S07	CS/ECE 5830 VLSI Architecture	3			🎓
S07	CS6712 Digital VLSI Testing	11			
S07	CS6967 Sp. Topics: Multithreaded Architecture	6			
F06	CS/ECE 6710 Digital VLSI	50			
F06	CS7940 HWRT Seminar	6			
S06	*Asynchronous Circuits*	*24*	*At Columbia Univ on sabbatical leave*		
F05	*Sabbatical leave*				
S05	CS/EE 6830 VLSI Architecture	19			
S05	CS6712 Digital VLSI Testing	8			
F04	CS/EE 5710 Digital VLSI	19			🎓
F04	CS/EE 6710 Digital VLSI	32			🎓
F04	CS/EE 6900 Architecture Seminar	3			
S04	CS/EE 5830 VLSI Architecture	12			🎓
S04	CS/EE 6830 VLSI Architecture	14			🎓
S04	CS6967 Digital VLSI Testing	5			
F03	CS/EE 5710 Digital VLSI	18			
F03	CS/EE 6710 Digital VLSI	38			
F03	CS/EE 6900 Architecture Seminar	3			
S03	CS/EE 5830 VLSI Architecture	10			
S03	CS/EE 6830 VLSI Architecture	12			
S03	CS6967 Digital VLSI Testing	5			
F02	CS/ECE 3710 Computer Design Lab	49			
F02	CS/EE 5710 Digital VLSI	15			
F02	CS/EE 6710 Digital VLSI	43			
S02	CS6964 VLSI Testing	6			
S02	CS6943 Sp. Topics: Asynchronous Systems	14			🎓
S02	CS/EE 3700 Digital System Design	135			🎓
F01	CS/EE 5710 Advanced I.C. Design	33			
F01	CS/EE 6710 Advanced I.C. Design	27			
S01	CS/EE 5830 VLSI Architecture	25			🎓
S01	CS/EE 6830 VLSI Architecture	13			🎓
F00	CS/EE 3710 Computer Design Lab	43			🎓
F00	CS/EE 5810 Adv. Computer Architecture	16			🎓
F00	CS/EE 5810 Adv. Computer Architecture	46			🎓
S00	CS/EE 3700 Digital System Design	130			
S00	CS4500 Software Engineering Projects *Team-Taught with Kessler & Henderson*	75			
F99	CS/EE 5810 Adv. Computer Architecture	6			
F99	CS/EE 6810 Adv. Computer Architecture	26			
S99	*Sabbatical leave*				
F98	*CSE 467 Adv. Digital Logic*	*24*	*At Univ. of Washington on sabbatical leave*		

Quarter	Course	Enrolled	Top 15%
Quarter System: Autumn, Winter, and Spring quarters			
S98	CS367 Computer Design Lab	43	🎓
W98	CS568 VLSI Architecture	15	🎓
W98	CS682 ASIC Seminar *(with Ganesh)*	3	
A97	CS361 Hardware Fundamentals	104	🎓
A97	CS685 ASIC Seminar *(with Ganesh)*	2	
S97	CS367 Computer Design Lab	26	🎓
W97	CS568 VLSI Architecture	17	
W97	CS685 ASIC Seminar	2	
A96	CS361 Hardware Fundamentals	108	🎓
A96	ASIC Seminar *(with Ganesh)*	2	

- Classes taught in years 1990-1996 (quarter system) are summarized in the following table. Scores are based on a formula used by the Dean's office to condense student evaluations into a single number. Top 15% cutoff and median values are based on scores from all classes taught in the College of Engineering.

Date	Course Number	Course Name	Class Size	My Evals	Top 15% Cutoff	Median
Spring 96	CS367	Computer Design Lab	40	**1.11** 🎓	1.11	0.30
	CS682	ASIC Seminar (with Ganesh)	5			
Winter 96	CS568	VLSI Architecture	15	0.61	1.13	0.45
	CS685	Async Seminar	2			
Autumn 95	CS361	Hardware Fundamentals	85	0.70	1.12	0.23
	CS685	ASIC Seminar (with Ganesh)	2			
Spring 95	CS572	High Level Synthesis: VHDL	21	0.69	1.18	0.41
	CS682	ASIC Seminar (with Ganesh)	5			
	CS685	Async Seminar	1			
Winter 95	CS365	Hardware Fundamentals	86	0.87	1.20	0.45
	CS682	ASIC Seminar (with Ganesh)	2			
	CS685	Async Seminar	5			
Autumn 94	CS568	VLSI Architecture	10	**1.62**🎓	1.00	.39
	CS685	ASIC Seminar (with Ganesh)	2			
Spring 94	CS544	Advanced VLSI Design	14	**1.26** 🎓	1.13	.32
	CS545	Testing Integrated Circuits	5	Evaluated with CS544		
	CS682	ASIC Seminar (with Ganesh)	4			
	CS685	Async Seminar	1			
Winter 94	CS365	Hardware Fundamentals	91	.91	1.17	.29
	CS682	ASIC Seminar (with Ganesh)	4			
	CS685	Async Seminar	1			
Autumn 93	CS568	VLSI Architecture	12	**1.25**🎓	1.14	.21
	CS685	ASIC Seminar (with Ganesh)				
Spring 93	CS562	Parallel Computer Organization	7	.25	1.12	.32
	CS682	ASIC Seminar (with Ganesh)	2			
	CS685	Async Seminar	3			
Winter 93	CS365	Hardware Fundamentals	87	**1.33** 🎓	1.22	.36
	CS682	ASIC Seminar (with Ganesh)	1			
	CS685	Async Seminar	5			
Autumn 92	CS571	VLSI Architecture	15	**1.12**🎓	1.12	.36
	CS682	ASIC Seminar (with Ganesh)				

Date	Course Number	Course Name	Class Size	My Evals	Top 15% Cutoff	Median
Spring 92	CS562	Parallel Computer Organization	10	**1.05** 🎓	1.01	.25
	CS682	ASIC Seminar (with Ganesh)	3			
	CS685	NSR Seminar	3			
Winter 92	CS561	Adv. Computer Organization	31	.88	1.16	.18
	CS682	ASIC Seminar (with Ganesh)	5			
Autumn 91	CS572	VLSI Architecture	14	Results lost by Dean's office		
	CS682	ASIC Seminar (with Ganesh)	2			
Spring 91	CS562	Parallel Computer Organization	6	.47	1.24	.30
	CS682	ASIC Seminar (with Ganesh)	3			
Winter 91	CS561	Adv. Computer Organization	26	.71	1.1	.42
	CS684	ASIC Seminar (with Ganesh)	5			
Autumn 90	CS572	VLSI Architecture	10	1.05	1.07	.28
	CS682	ASIC Seminar (with Ganesh)	2			

Courses Developed

UGS/CS 2050 — Making Noise: Sound Art and Digital Media — As part of my University Professorship I developed this new undergraduate course on the theme of *technological fluency*. This course was initially offered during the Spring semesters in 2015 and 2016 as part of the General Education program. It has subsequently been offered again in Spring 2018. This course introduces students from across campus to a variety of digital media subjects that also involve computation. I emphasize hands-on projects that include both programming and physical/electronic artifacts. Essentially this is a way to introduce students to computing and increase their technological fluency but through digital media projects rather than engineering projects. It is also a way to expand students' ideas about technology in the arts and how arts and technology interact in our modern world. This is a lower-division course that will serve a variety of General Education purposes, and will culminate with a public presentation of student projects.

CS6965/6958 — Hardware Ray Tracing — A special topics class first taught in Fall 2012, and again in Spring 2014, and Spring 2015 (offered in 2015 by my graduate students, Daniel Kopta and Konstantin Shkurko), this class explores ray tracing as a commuter graphics rending technique and how the algorithm interacts with special purpose hardware. Students implement ray tracing software and run that application on a simulation of a special-purpose architecture for graphics processing developed by my research group. Through this exploration students get experience not only with the practice of computer architecture research, but first-hand experience in proposing architectural changes to support specific algorithms.

CS5789 — Embedded Systems and Kinetic Art — First taught in the fall of 2009, and now in its 6th offering in Spring 2019, this course was developed as a collaborative course with Professor Paul Stout in the Department of Art and Art History. The aim is to pair embedded systems students (mostly Computer Science and Computer Engineering students) with Art students (mostly sculpture majors) to make kinetic art projects. Kinetic art is art that uses motion, light, or sound as part of its realization. In practice many kinetic art projects use microcontrollers to control the kinetic aspect of the art. The aim of this class is to enhance the creative problem solving skills of the engineers, and the engineering skills of the artists through the group projects.

CS/Art 5965/6965 — VLSI and Art — A special topics course taught in the Fall of 2007, this course was developed as a cooperative course with Professor Justin Diggle in the Department of Art and Art History. The plan was to get artists (printmakers in particular) together with engineers (VLSI chip designers in particular) to do joint projects involving integrated circuits and art. A Teaching Committee grant was received for this collaborative course for $7075 which was used to buy a large format printer to support the course.

CS 6967 — Multithreaded Computer Architecture — A special topics course in Spring 2007. This is a project-based special topics course to study multithreaded approaches to computer architecture. This course led to the architectural simulation infrastructure that we are still using in my Hardware Ray Tracing research group.

CS/EE 5830/6830 — VLSI Architecture — This is a new course from Spring 2005 on digital computer arithmetic. It was developed from the ground up to study high-performance arithmetic circuits in detail: adders, multiple argument addition, multiplication, division, square root, etc.

CS/EE 6712 — Digital VLSI Testing — A course where students test the chips that they designed in 5710/6710.

Because students can fabricate their chips in 5710/6710, a course is needed in the spring in order to test those chips. We use the dedicated LV500 test hardware for this lab class.

CS/EE 5710/6710 — Digital VLSI Design — After Prof. Kent Smith's retirement in spring 2001, I took over this course and completely restructured it. This course now involves a major project, uses CAD tools from Cadence and Synopsys, and has a strong emphasis on building large VLSI systems. It also allows students to fabricate their projects as integrated circuits. During my sabbatical in Spring 2006 I wrote the first draft of a new VLSI CAD Manual textbook for this course. It has subsequently been published by Addison-Wesley.

CS/EE 5810/6810 — Restructured this Advanced Computer Architecture course in the Fall of 2000 to use a lab-based approach where students build a timing simulator of a pipelined, out-of-order, branch predicting machine along with the discussions in the book.

CS4500 — Senior Software Lab — Bob Kessler, Tom Henderson, and I restructured this course in Spring 2000 to be a project-driven course with individual group meetings rather than lectures. We also included a design contest with judges and prizes from local companies. The result was a great success.

CS361-2-3 (Now CS3700-3810) — Digital Logic — Helped restructure the sophomore digital logic sequence. This sequence was formerly numbered 364-5-6. The sequence has been changed to be bottom-up starting with digital design in the fall, and moving up to computer systems in the spring. A new book was used, and the curriculum has been changed to be consistent across the three classes in the sequence. This change allows students to build much more significant circuit projects than in the past because they start building circuits in the fall, and continue through spring. In the older version the lab kits were used only in winter and spring quarters.

CS367 (Now CS3710) — Computer Design Lab — Redesigned the sophomore digital design lab course to involve designing and building a realistic computer processor. Xilinx and Actel FPGA are used so that the students can build designs that are much larger, more realistic, and complex than previously possible in this class.

CS365 — Restructured the basic digital logic class around the use of new commercial CAD tools from VIEW*logic* and also introduced Xilinx FPGAs into the lab portion of the class. The entire 300-level hardware series will be restructured starting in Fall 1995 using a bottom-up approach starting with digital logic in the fall, and ending with the hardware/software interface in the spring.

Special Topics, VHDL — This course was developed to teach high-level hardware synthesis using the VHDL language. This is an industry standard hardware description language and is used through the VIEW*logic* tools, and other new CAD tools now available to our classes. It was developed as part of the Advanced VLSI course taught in Spring 1994. It was taught again as a special topics course in Spring 1995.

CS568 (now CS/EE 5830/6830) — HDL Design — Developed a new course to let students investigate the mapping of computer architecture into VLSI through the use of Field Programmable Gate Arrays (FPGAs). Students design VLSI systems and implement them in the same quarter using Actel FPGA technology.

CS561 — Advanced Computer Architecture — Designed course around a new book (Hennessey and Patterson, Computer Architecture: A Quantitative Approach). This course emphasizes quantitative aspects of computer architecture by using measurements of machine usage as a guide to developing advanced computer architectures.

CS562 — Parallel Computer Architecture — Developed course to teach students about the architecture of parallel machines. Case studies of existing parallel computers are used to illustrate different design decisions.

CS685 — Asynchronous Systems — This course allows students to explore individual ideas related to asynchronous circuits and systems.

SERVICE

National Science Foundation

- Starting in September 2019, I took a leave from the University of Utah to accept a three-year position at the National Science Foundation (NSF) as a Program Director. I was a Program Director in CISE/CNS (Computer and Network Systems), specifically in the Computer Systems Research (CSR) program (2019-2022). Since then I have been a part time (one day a week) Program Director and will continue in that role through August 2024 .
- Since 1997 I have averaged 1-2 NSF panels per year in a variety of programs

Professional Societies

Senior Member, ACM

- Member of SIGCSE, SIGGRAPH
- Member of ACM Distinguished Speaker Program *2015 — present*

Senior Member, IEEE

- Member of Computer Society, Technical Committee on VLSI

Reviewing

Referee for: ACM SIGGRAPH, ACM SIGCSE, High Performance Graphics conference, Great Lakes Symposium on VLSI, IEEE Symposium on Asynchronous Circuits and Systems, Impact printmaking conference, Proceedings of the IEEE, Formal Methods in System Design, Harper Collins, IEEE Design and Test of Computers, IEEE Transactions on Computers, IEEE Transactions on Computer Aided Design, IEEE Transactions on VLSI, IEE Journal on Computers and Digital Techniques, International Journal of Parallel Programming, Journal of VLSI Signal Processing, Klewer Academic Publishers, National Science Foundation (1-2 panels per year on average), National Conference on Undergraduate Research (All C.S. related submissions for the 1993 conference). Prentice-Hall, And many others I've forgotten about...

Conference Organization

- Conference Chair for ACM SIGGRAPH 2023 - Held in Los Angeles in August 2023 (14,275 attendees).
- General Co-Chair (with Ken Stevens) of the 2020 IEEE International Symposium on Asynchronous Circuits and Systems, May 2020, Salt Lake City, UT (VIrtual Event)
- ACM SIGGRAPH Labs Co-Chair (WIth Forest Lucas), 2020, Washington, D.C., August 2020 (organizing a four-day hands-on studio mini-conference during SIGGRAPH)(Virtual Event)
- ACM SIGGRAPH Education Chair, 2017, 2018 (organized and curated a two-day mini-conference on education, the Educator's Forum, at SIGGRAPH)
- General co-Chair (with Ken Stevens) of the 2012 ACM Great Lakes Symposium on VLSI (GLSVLSI), held in Salt Lake City, UT, May 2012.
- General Chair of the 2011 IEEE International Symposium on Asynchronous Circuits and Systems (Async 2011) held in Ithaca, New York in April 2011
- Technical Program co-Chair (With Ken Stevens) of the Great Lakes Symposium on VLSI (GLSVLSI) 2010.
- General Chair of the 2001 IEEE International Symposium on Asynchronous Circuits and Systems (Async 2001) held in Salt Lake City in March, 2001.
- General Chair and co-Program Chair (with Chris Myers) of the 2001 Conference on Advanced Research on VLSI, held in Salt Lake City in March, 2001.
- Co-General Chair (with Al Davis) for the 1994 International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async94), held in Salt Lake City in November 1994.

Conference Committees

- ACM SIGGRAPH Conference Advisory Group (steering committee for SIGGRAPH Conference), 2023 - present.
- Steering Committee for ACM Great Lakes Symposium on VLSI (GLSVLSI), 2012 — present.
- Chair, ACM SIGGRAPH Distinguished Educator Award committee, 2018—2021.
- Member of the ACM SIGGRAPH Art Gallery Jury (program committee), 2019.
- Member of the Program Committee, ACM Symposium on Microelectronic Systems Education, Washington D.C., 2019.
- Member of the ACM SIGGRAPH General Submissions Program Committee, 2014, 2015, 2017, 2018, 2019, 2022.
- Member of the Steering Committee for the IEEE International Symposium on Asynchronous Circuits and Systems, 1996–2011, 2014–present (Chair, 1996–2011)
- Member of the program committee for the IEEE International Symposium on Asynchronous Circuits and Systems, 1994, 1996, 1997, 1998, 1999, 2000, 2003, 2004, 2005, 2006, 2007, 2009, 2010, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2021, 2022, 2023.
- Publication chair for the International Symposium on Advanced Research in Asynchronous Circuits and Systems 1997, 1998, 2000, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018.
- Publication Chair for the 2008 High Performance Computer Architecture (HPCA) conference to be held in Salt Lake City.
- Member of Program Committee for ACM/Eurographics High Performance Graphics, 2009, 2010, 2011, 2012, 2013, 2014.
- Member of Program Committee for IEEE Symposium on Interactive Ray Tracing (RT), 2006, 2007, 2008.
- Member of the program committee for the ACM Great Lakes Conference on VLSI (GLSVLSI), 2003, 2005, 2006 (track co-chair), 2009 (track co-chair).
- Member of the program committee for the 20th Anniversary Conference on Advanced Research in VLSI, Georgia Institute of Technology, March 1999.
- Member of the program committee for the IEEE International Conference on Computer Design (ICCD) 1995, 1996, 1997.
- U.S. academic representative for the 1996 International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async96), Aizu, Japan, March 1996.
- Member of the program committee for the 6th NASA Symposium on VLSI, Albuquerque, New Mexico, January 1995.
- Coordinator (with Ganesh Gopalakrishnan) of a day-long "minitrack" on asynchronous circuits and systems, 26th Hawaii International Conference on System Sciences, January 5-8, 1993.
- Member of the program committee for the International Workshop on Field Programmable Logic and Applications:
  - — 1993, Oxford University, England
  - — 1994, Prague, The Czech Republic
  - — 1995, Oxford University, England

University Academic Committees

- External Review Committee for the DXARTS Program, University of Washington, Seattle, WA, January 2018.
- University Teaching Committee
  - — Chair 2015–2019
  - — Member 2013–2014
  - — Chair 2001–2005
  - — Member 1999–2001
- Graduate School Review Committee for the Department of Film and Media Studies, 2014.
- Creative Campus Steering Committee, 2012–2015
- University Research Committee, 2006–2009
- University Conflict of Interest Committee, 2000–2002.
- Bachelor of University Studies Committee, 1996–1998.
- Graduate School Review Committee for the Department of Parks, Recreation and Tourism, 1997.

- University of Utah Faculty Club:
  - — President 1995-1996
  - — Vice President 1994-1995
  - — Treasurer 2008–2010
  - — Member of the Board of Directors, 1992–1994, 1999–2014.

College Academic Committees

- Curriculum Committee, 2011–2018
- ABET Committee, 2006–2012
- Director of the Computer Engineering Program (an ABET-accredited BS degree granting program in the College of Engineering): 1993–1997, 2002–2005, 2009–2012, 2015–2018.
- RPT Committee, 1999–2001.
- Computing Committee, 1999–2000.
- Chair of Academic Appeals Committee, 1998–1999.
- College Council, 1991–1994.

School of Computing Academic Committees

- Retention, Promotion, and Tenure (RPT) Committee Chair, 2022 – 2024
- Director of the Computer Science Grad Degree Track, 2021-2022
- Chair, Lecturing Faculty Recruiting Committee, 2018-2019
- Director of Computing Degree Track in Computer Engineering, 2007–2022
- Member, Computer Engineering Track Faculty 2007 – present
- Member, HCC Track Faculty 2017 – present
- Director of Computing Degree Track in Digital Media, 2011–2015 (track put on hiatus)
- Director of Graduate Studies. 1997–1998, 2007–2009
- Director of Graduate Admissions, 1995–1997, 2006–2007
- Curriculum Committee, 2011–present.
- Scholarship Committee, 2014–present.
- Graduate Admissions Committee, 1999–2000, 2008–2014.
- Department RPT Chair, 2001–2003.
- Chair of Computing Policy Committee, 1999–2000.
- Member, Graduate Studies Committee, 1995–1996, 2006–2007, 2010–present.
- Semester Conversion Committee, 1997–1998.
- Computer Engineering Committee
  - — Chair, 1993–1997, 2002–2005, 2009–2012, 2015–2018
  - — Member, 1992–1993, 1999–2002, 2006–2009, 2012–2015, 2018-present

- Chair of Hardware Comprehensive Exam Committee, 1999, 2000.
- Member, Graduate Comprehensive Exam Committee, 1996, 1998, 2001, 2002.
- Faculty Recruiting Committee, 1992 — 1993.