Chris John Myers

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Education

Stanford University, Stanford, California (1991-1995)

Ph.D. degree in Electrical Engineering (1995)
Thesis: Computer-Aided Synthesis and Verification of Gate-Level Timed Circuits

M.S. degree in Electrical Engineering (1993)

California Institute of Technology, Pasadena, California (1987-1991)

B.S. degree with honor in Electrical Engineering and History (1991)

Professional Experience

Chair of Elec., Comp., and Energy Eng., *University of Colorado Boulder* (2020-present)
Professor of Elec., Comp., and Energy Eng., *University of Colorado Boulder* (2020-present)
Affiliated Professor of Biomedical Engineering, *University of Colorado Boulder* (2020-present)
Affiliated Professor of Computer Science, *University of Colorado Boulder* (2020-present)
Associate Chair of Electrical and Computer Engineering, *University of Utah* (2018-2020)
Professor of Electrical and Computer Engineering, *University of Utah* (2006-present)
Adjunct Professor of Computer Science, *University of Utah* (2007-present)
Adjunct Professor of Bioengineering, *University of Utah* (2007-present)
Visiting Professor of Engineering Science, *University of Oxford* (summer 2019)
Visiting Professor of Electrical and Computer Engineering, *Boston University* (2017)
Visiting Professor of Computer Science, *Newcastle University* (2016-2017)
Director of Computer Engineering, *University of Utah* (2000-2002, 2006-2009)
Adjunct Associate Professor of Computer Science, *University of Utah* (2003-2007)
Adjunct Associate Professor of Bioengineering, *University of Utah* (2003-2007)
Associate Professor of Electrical and Computer Eng., *University of Utah* (2001-2006)
Visiting Scholar, *Tokyo Institute of Technology* (summer 2003)
Visiting Scholar, *Stanford University* (2002-2003)
Research Assistant Professor of Computer Science, *University of Utah* (1996-2003)
Director of the Center for Asynchronous Circuit Design, *University of Utah* (1997-2001)
Assistant Professor of Electrical Engineering, *University of Utah* (1995-2001)
Consultant, Intel Corporation, Portland, Oregon, (1996-1998)
Consultant, Intel Corporation, Haifa, Israel, (summer 1995)
Research Assistant, Professor Teresa Meng, *Stanford University* (1991-1995)
Teaching Assistant, Professor Charles Seitz, *California Institute of Technology* (1990-1991)
Research Assistant, Professor James Lee, *California Institute of Technology* (1989-1991)
Software Engineer, Business Data Systems, Billings, Montana (1985-1989)

Awards

Fellow of the IEEE (2013)

ECE Departmental Service Award, *University of Utah* (2013)

Best Paper Award, Symposium on Asynchronous Circuits and Systems (2007)

Best Paper Award Finalist, Symposium on Asynchronous Circuits and Systems (2001)

Best Paper Award, Symposium Asynchronous Circuits and Systems (1999)

Teaching commendation for CS/EE 5740, *University of Utah* (1998)

National Science Foundation CAREER Award (1996)

National Science Foundation Graduate Fellowship (1991)

Rodman W. Paul History Prize, *California Institute of Technology* (1991)

Tau Beta Pi National Honor Society (1991)

Carnation Merit Award, *California Institute of Technology* (1990)

First Prize VLSI Design Contest, *California Institute of Technology* (1990)

Grant Activities

1. C. Myers, "Accelerating Synthetic Biology Discovery & Exploration through Knowledge Integration", October 2019 - September 2021, National Science Foundation, $204,296.
2. C. Myers, "An Efficient Framework for the Stochastic Verification of Computation and Communication Systems Using Emerging Technologies", July 2019 - June 2023, National Science Foundation, $346,000.
3. C. Myers, "Genetic circuit design for extreme environments enabled by models extracted from petabyte+ perturbation analyses", July 2018 - August 2021, DARPA, $308,353.
4. C. Myers, "NSF Student Travel Grant for 2018 Computational Modeling in Biology Network (COMBINE) Forum", May 2018 - May 2019, National Science Foundation, $10,000.
5. C. Myers, "NSF Student Travel Grant for 2018 Hackathons on Resources for Modeling in Biology (HARMONY)", May 2018 - May 2019, National Science Foundation, $10,000.
6. C. Myers, "Evolvable Living Computing - Understanding and Quantifying Synthetic Biological Systems' Applicability, Performance, and Limits", August 2017 - August 2018, National Science Foundation (sub-award from Boston University), $41,266.
7. C. Myers, "A Standard Enabled Workflow for Synthetic Biology", August 2017 - August 2019, National Science Foundation, $150,000, REU supplements totaling $31,758.
8. C. Myers, "Student Travel Support for COMBINE 2016", June 2016 - May 2017, National Science Foundation, $15,000.
9. C. Myers, "Student Travel Support for SBOL 14 Workshop", March 2016 - March 2017, National Science Foundation, $10,000.
10. C. Myers, "Student Travel Support for COMBINE 2015", June 2015 - May 2016, National Science Foundation, two awards totally $16,000.
11. C. Myers, H. Sauro (UW), and J. Gennari (UW), "Synthetic Biology Open Language Resource", July 2014 - June 2018, National Science Foundation, $444,527 (Utah share).
12. C. Myers, "Student Travel Support for HARMONY 2015", July 2014 - June 2015, National Science Foundation, $10,000.

13. C. Myers, "Genetic Design Automation", July 2012 - June 2015, National Science Foundation, $449,980, REU supplements totaling $32,000, travel supplement $15,000.

14. C. Myers and P. Li (TAMU), "Integrated Verification, Built-in Self-test, and Tuning for Digitally-Intensive Analog Systems", July 2011 - July 2014, Nat. Sci. Foundation, $224,998 (Utah share).

15. C. Myers, "Simulation Aided Verification of AMS Circuits", May 2010 - January 2011, Intel Corporation, $35,000.

16. C. Myers and H. Zheng (USF), "Methods and Tools for the Verification of Cyber-Physical Systems", September 2009 - August 2012, National Science Foundation, $270,000 (Utah share).

17. C. Myers and C. Winstead (USU), "Soft-Logic Modeling and Design for Synthetic Biology", July 2009 - June 2012, National Science Foundation, $262,000 (Utah share).

18. C. Myers, "Simulation Aided Verification of AMS Circuits", October 2008 - September 2011, Semiconductor Research Corporation, $198,864.

19. C. Myers, "Designing Reliable Systems Using Unreliable Components", July 2007 - June 2009, National Science Foundation, $150,000.

20. C. Myers, "Formal Verification of Analog and Mixed-Signal Circuits", October 2005 - September 2008, Semiconductor Research Corporation, $270,000.

21. C. Myers, "A Principled Mapping of Regulatory Networks to Asynchronous Circuit Models for Stochastic Analysis", September 2003 - August 2006, National Science Foundation, $425,864, REU supplement $5,000.

22. C. Myers, "System-Level Timing Verification with Automatic Abstraction", August 2002 - July 2005, Semiconductor Research Corporation, $270,000.

23. C. Myers, "U.S.-Japan Cooperative Science: Synthesis and Verification of High Performance Timed Circuits and Systems", April 2001 - April 2004, National Science Foundation, $30,000.

24. C. Myers, C. Schlegel (co-PI), R. Harrison (co-PI), "Design Methodology for Mixed Analog/Asynchronous VLSI Implementations of Communications Systems", September 1999 - August 2002, National Science Foundation, $300,000, REU supplement $5,000.

25. C. Myers, "Timing Verification using Automatic Abstraction", July 1999 - June 2002, Semiconductor Research Corporation, $174,000.

26. C. Myers, E. Brunvand (co-PI), "Center for Asynchronous Circuit and System Design", July 1999 - June 2000, State of Utah, $130,000.

27. C. Myers, "Synthesis and Verification of Timed Circuits", August 1997 - July 2000, Semiconductor Research Corporation, $150,000.

28. C. Myers, "Specification and Compilation Techniques for 1 GHz and Beyond", awarded May 1998, Intel Corporation, $20,000.

29. C. Myers, E. Brunvand (co-PI), "Center for Asynchronous Circuit and System Design", July 1998 - June 1999, State of Utah, $115,000.

30. C. Myers, E. Brunvand (co-PI), "Center for Asynchronous Circuit and System Design", July 1997 - June 1998, State of Utah, $100,000.

31. C. Myers, "Design Methods and Tools for Mixed-Timed Systems", July 1996 - June 2000, NSF CAREER Award, $210,000, U. of Utah matching grant $5,000, REU supplement $5,000.

Development Activities

1. Cash gift from Intel Corporation for research, Dec 2011, $28,000.
2. Cash gift from CEDA to support FAC workshop, June 2011, $3,000.
3. Cash gift from Intel to support FAC workshop, Dec 2010, $2,000.
4. Cash gift from SRC to support verification review, Dec 2006, $5,000.
5. Several cash gifts from SRC to support undergraduate research, May 2006, $6,000, Sept. 2005, $6,000, May 2005, $6,000, Sept. 2004, $6,000, May 2004, $6,000, May 2003, $12,000, Sept. 2002, $12,000, May 2002, $6,000, Aug. 2001, $18,000, May 2001, $12,000, Oct. 2000, $6,000.
6. Cash gift from SRC to support verification review, Dec 2001, $5,000.
7. Computer equipment donation from Intel Corporation, October 2000, valued at $20,000.
8. Software donation from VeriBest Incorporated, January 1999, valued at $2,250,000.
9. Cash gift from Intel Corporation for research, June 1997, $20,000.
10. Software donation from Intel Corporation, July 1996, valued at $1,100.
11. Cash gift from Intel Corporation for research, April 1996, $53,600.
12. Computer equipment donation from Intel Corporation, March 1996, valued at $12,756.
13. Cash gift from Intel Corporation for research, January 1996, $15,500.

Languages

Working knowledge of written and spoken Chinese.

Academic Service

BioFrontiers Council Member, *University of Colorado Boulder* (2020-present)
Computer Engineering Committee Member, *University of Utah* (1995-2016, 2018-2020)
Recruiting Committee Chairman, *University of Utah* (2001-2002, 2004-2006, 2017-2018)
Recruiting Committee Member, *University of Utah* (1995-2000, 2015-2016, 2018-2019)
Coordinator for Electrical Engineering Senior Projects, *University of Utah* (2011-2013)
Faculty Senate, *University of Utah* (2010-2013)
Computer Engineering Director, *University of Utah* (2000-2002, 2006-2009)
Organizer of Judd Distinguished Lecture Series, *University of Utah* (2005-2008)
Assessment and Planning Committee, *University of Utah* (2003-2004)
Strategic Goals Committee Member, *University of Utah* (1997-2001)
Curriculum Committee Member, *University of Utah* (1995-1998)
Computing Committee Member, *University of Utah* (1995-1998)
College Council Member, *University of Utah* (1995-1998)
Alumni Fund House Chair, *California Institute of Technology* (1994-1998)

Professional Activities

Member of the IEEE, S'91-M'96-SM'04-Fellow'13 (1991-present)
Member of the ACM (1996-present)
Chair, *Synthetic Biology Open Language* (2019-present)
Chair, *COMBINE (COmputational Modeling in Biology NEtworks) Coordination Board* (2019-present)
Member, *External Advisory Board for the BioDesign CDT*, *Imperial College London* (2019-present)
Technology Editor, *ACS Synthetic Biology* (2017-present)
Member of the Editorial Board, *Engineering Biology* (2016-present)
Member of the Editorial Board, *Synthetic Biology* (2016-present)
Int. Rep. on the SynBio CDT Directorate Comm., *Oxford University* (2016-present)
Member of the Portabolomics Advisory Board, *Newcastle University* (2016-present)
Member of the Steering Committee, *Synthetic Biology Open Language* (2015-present)
Member of the Steering Committee, *Synthetic Biology Standards Consortium* (2015-present)
Member, COMBINE (COmputational Modeling in Biology NEtworks) Coordination Board (2014-present)
Member of the Steering Committee, *Frontiers in Analog CAD Workshop* (2010-present)
Associate Editor, *IEEE Life Sciences Letters*, (2014-2017)
Guest Editor, *IEEE Design & Test Magazine* (2015-2016)
Organizer, *COMBINE Forum 2015* (2015)
Member of the Editorial Board, *Frontiers in Synthetic Biology* (2013-2015)
Associate Editor, *IEEE Transactions on VLSI* (2009-2014)
Member of the Editorial Board, *Formal Methods in System Design* (2006-2014)
Guest Editor, *ACM Journal of Emerging Technologies in Computing Systems*, (2013-2014)
Associate Editor, *IEEE Design and Test Magazine*, (2012-2014)

Editor, *Systems Biology Markup Language* (SBML) (2011-2013)
Guest Editor, *ACS Synthetic Biology*, (2013)
Member of the Review Panel, *NIH MABS Study Section* (2012)
Simulation and Verification Track Chair, *Int. Conf. on Computer-Aided Design* (2012)
Publications Chair, *Int. Workshop on Bio-Design Automation* (2012)
Co-Program Chair, *Frontiers in Analog CAD Workshop* (2011)
Site Reviewer, *NSF Expeditions* (2011)
Member of the Best Paper Committee, *Async. Circuits and Systems Conf.* (2006, 2008)
Organizer, *SRC Verification Review* (2002, 2007)
Co-organizer and Technical Program Chair, *Asynchronous Circuits and Systems Conf.* (2001)
Co-organizer and Technical Program Chair, *Advanced Research in VLSI Conf.* (2001)
Tools Chair, *Asynchronous Circuits and Systems Conference* (1998)
Member of the PC, *Async Ckts/Sys Conf.* (1998-2004, 2006, 2008-2009, 2011, 2017-present)
Member of the PC, *Conference on Analysis and Design of Hybrid Systems* (2017-present)
Member of the PC, *Winter Simulation Conference* (2017-present)
Member of the PC, *Workshop on Hybrid Systems and Biology* (2013-present)
Member of the PC, *Int. Conf. on Formal Modeling and Analysis of Timed Sys.* (2010-present)
Member of the PC, *Int. Workshop on Bio-Design Automation* (2009-present)
Member of the PC, *Frontiers in Analog CAD Workshop* (2005-present)
Member of the PC, *ACM Int. Conf. on Nanoscale Comp. and Comm.* (2016, 2018)
Member of the PC, *IJCAI 2016 Workshop: AI for Synthetic Biology* (2015-2016)
Member of the PC, *Symposium on Theory of Modeling and Simulation* (2014-2017)
Member of the PC, *Forum on Specification and Design Languages* (2011-2016)
Member of the PC, *Workshop on Modeling of Biological Systems*, (2013)
Member of the PC, *ICNC Workshop on Cyber-Physical Systems* (2013)
Member of the PC, *ISMB SIG on Biological System Design* (2012)
Member of the PC, *Int. Conf. on Bioinfo., Biocomp. Sys., and BioTech.* (2011-2012)
Member of the PC, *Great Lakes Symposium on VLSI* (2010-2012)
Member of the PC, *Int. Conf. on Computer-Aided Design* (2009-2012)
Member of the PC, *Virtual Worldwide Forum on Electronic Design Automation*, (2011)
Member of the PC, *Logic Aspects of Fault Tolerance*, (2009, 2011)
Member of the PC, *Int. Conf. on Computational and Systems Biology* (2010)
Member of the PC, *Int. Conf. on Information Technology* (2007)
Member of the PC, *Conf. on Information Technology* (2006)
Member of the PC, *Formal Methods for GALS* (2003, 2005)
Member of the PC, *Computer Aided Verification Conference* (2003-2004)
Member of the PC, *Workshop on Theory and Practice of Timed Systems* (2002)
Panelist, numerous *NSF Review Panels*
Reviewer, *Morgan Kaufman, McGraw Hill, Wiley, Hong Kong Univ. Grants, many IEEE journals*

Graduated Students (Committee Chairman)

PhD - Tramy Nguyen - Asynchronous Genetic Circuit Design, 9/19.
PhD - Leandro Watanabe - Modeling and Simulation for Heterogeneous Populations, 12/18.
PhD - Zhen Zhang - Verification Methodologies for Fault-Tolerant NoC Systems, 12/15.
PhD - Andrew Fisher - Efficient, Sound Formal Verification for AMS Circuits, 8/15.
PhD - Nicholas Roehner - Technology Mapping of Genetic Circuit Designs, 8/14.
PhD - Curtis Madsen - Stochastic Analysis of Synthetic Genetic Circuits, 8/13.
PhD - Robert Thacker - A New Verification Method For Embedded Systems, 12/10.
PhD - Scott Little - Efficient Modeling and Verif. of AMS Circuits Using LHPNs, 8/08.
PhD - Nathan Barker - Learning Genetic Reg. Net. Connectivity from Time Series Data, 8/07.
PhD - Hiroyuki Kuwahara - Model Abs. & Temp. Behv. Analysis of Genetic Reg. Net., 8/07.
PhD - David Walter - Verification of AMS Circuits Using Symbolic Methods, 8/07.
PhD - Curt Nelson - Technology Mapping of Timed Cirucits, 12/04.
PhD - Hans Jacobson - Interlocked Synchronous Pipelines, 12/03.
PhD - Eric Mercer - Correctness and Reduction in Timed Circuit Analysis, 12/02.
PhD - Jie Dai - Design Methodology for Analog VLSI Impl. of Error Control Decoders, 12/02.
PhD - Eric Peskin - Protocol Selection, Impl., and Analysis for Asynchronous Circuits, 8/02.
PhD - Hao Zheng - Modular Syn.&Verif. of Timed Circuits Using Automatic Abstraction, 8/01.
PhD - Wendy Belluomini - Algorithms for Synthesis and Verification of Timed Circuits, 9/99.
MS - Pedro Fontanarrosa, Automated Generation of Dynamic Models for GRNs, 6/19.
MS - Michael Zhang, SBOLExplorer: Data Mining for Genetic Design Repositories, 4/19.
MS - Meher Samineni, Software Compliance Testing for Workflows using SBOL, 8/18.
MS - Dhanashree Kulkarni, Improved Model Gen. and Prop. Spec. for AMS Circuits, 8/13.
MS - Satish Batchu - Automatic Extraction of Behv. Models from Sim. of AMS Circuits, 12/10.
MS - Nam Nguyen - Design and Analysis of Genetic Circuits, 8/08.
MS - Yanyi Zhao - Application of Sync Synthesis Tools for High-Level Async Design, 12/04.
MS - Chris Krieger - Complete State Coding of Timed Asynchronous Circuits, 12/02.
MS - Kip Killpack - Analysis and Characterization of a Locally-Clocked Module, 5/02.
MS - Robert Thacker - Implicit Methods for Timed Circuit Synthesis, 6/98.
MS - Hao Zheng - Specification and Compilation of Timed Systems, 6/98.
MS - Brandon Bachman - Architectural-Level Synthesis for Asynchronous Systems, 9/98.
MS - Eric Mercer - Stochastic Cycle Period Analysis in Timed Circuits, 5/99.
BS - Michael Zhang, SBOLDesigner: A Hierarchical Genetic Design Editor, 4/18.
BS - Meher Samineni, Software Compliance Testing for SBOL, 8/17.
BS - Leandro Watanabe - Hierarchical Stochastic Simulation Algorithm, 5/14.
BS - Tyler Patterson - Modeling and Visualization of Genetic Circuits, 5/11.
BS - Kevin Jones - Automated Abstraction of Labeled Petri Nets, 5/11.
BS - Scott Little - Comparative Study of Several Timing Analysis Algorithms, 5/03.
BS - Yanyi Zhao - An Aysnchronous MPEG Ditherer, 5/03.
BS - Allen Sjogren - Interfacing Synchronous and Asynchronous Modules, 5/98.
BS - Jeff Cuthbert - XATACS: The Next Generation in Asynchronous Circuit Design, 5/98.

Current Graduate Students (Committee Chairman)

PhD - Jeanet Mante, Biomedical Engineering, University of Colorado Boulder

PhD - Lukas Bucherl, Biomedical Engineering, University of Colorado Boulder

PhD - Pedro Fontanarrosa, Biomedical Engineering, University of Utah

MS - Logan Terry, Computer Science, University of Utah

Postdocs Supervised

Zhen Zhang - libSBOLj: A Java Library for SBOL (2015-2016)

Jian Wu - Analysis of Network-on-Chip Routing Protocols (2010-2011)

Sung-tae Jung - Direct Synthesis of Timed Circuits (1999-2000)

Undergraduate Projects Supervised

Payton Thomas - iBioSim (current)

Benjamin Hatch - VisBOL and SynBioHub3 (current)

Eric Yu - SBOLExplorer and SynBioHub3 (current)

James Scholz - SynBioHub Testing (current)

CS Capstone Design Team (2019-2020)

Oliver Flatt - SynBioHub Testing

Samuel Bridge - SBOLDesigner

Nathan Wilkinson - VisBol

Igor Durovic - SBOL Library

Zach Zundel - SynBioHub

Tramy Nguyen - SBOL Library

Scott Glass - Flux Balance Analysis

Jason Stevens - Dynamic Modeling of Genetic Circuits

Hill Air Force clinic (2003-2008)

Curtis Madsen - Engineering Scholars Program

Nick Seegmiller - Engineering Scholars Program

Kip Killpack - A Low Power Digital Hearing Aid

Eric Mercer - SPAM Microprocessor Simulator

Brandon Bachman - SPAM Microprocessor Simulator

Robert Thacker - SPAM Microprocessor

Courses Taught

Modeling and Analysis of Biological Networks (2003,2005,2007,2010,2013,2015,2017,2018)

Computer Design Laboratory (1999,2001,2012,2014,2019)

Fundamentals of Digital System Design (1999,2001,2014,2016,2019)

Asynchronous Circuit Design (1995,1997,2000,2001,2004,2006,2009,2011,2013,2015)

Formal Verification (1997,2012)

Embedded System Design (2004-2007, 2011)

Case Studies in CES (2008)

CE Junior Seminar (2006-2008,2018)

Hill Air Force Clinic (2003-2008)

CE Senior Thesis (2002)

Computer Aided Design of Digital Circuits (1996,1998,2000)

Hardware Fundamentals: Computer Organization and Design (1997-1998)

Microprocessor Laboratory (1996)

Courses Developed

1. Modeling and Analysis of Biological Networks - In 2009, I published the textbook, *Engineering Genetic Circuits*, used for this course.
2. Asynchronous Circuit Design - In 2001, I published the textbook, *Asynchronous Circuit Design*, used for this course.
3. Computer Aided Design of Digital Circuits - This course provides an introduction to algorithms for the synthesis and optimization of digital designs.
4. Embedded System Design - I completely redesigned this course to focus on embedded system design issues rather than just interfacing with a PC.
5. Hardware Fundamentals - I completely redesigned a core course on hardware fundamentals and computer organization including adding new material to teach VHDL.
6. Formal Verification - This course presents state-of-the-art methods for the formal verification of hardware and software systems. A new version of this class was developed in 2012.

Publications and Patents

Books

1. C. J. Myers (translated by Li), *Asynchronous Circuit Design* (in Chinese), Tsinghua University Press, September, 2013.
2. C. J. Myers, *Engineering Genetic Circuits*, Chapman & Hall/CRC Press, July, 2009.
3. C. J. Myers (translated by T. Yoneda), *Asynchronous Circuit Design* (in Japanese), Kyoritsu Shuppan, September, 2003.
4. C. J. Myers, *Asynchronous Circuit Design*, John Wiley and Sons, July, 2001.
5. J. Z. Lee, C. Campbell, and C. J. Myers, *Fate and Fortune in Rural China: Social Structure and Population Behavior in Liaoning*, Cambridge University Press, 1997.

Book Chapters and Books Edited

1. T. Neupane, Z. Zhang, C. Madsen, H. Zheng, and C. Myers, "Approximation techniques for stochastic analysis of biological systems", in *Automated Reasoning for Systems Biology and Medicine*, pages 327-348, 2019.
2. C. Myers, K. Clancy, G. Misirli, E. Oberortner, M. Pocock, J. Quinn, N. Roehner, and H. Sauro, "The Synthetic Biology Open Language", in *Computational Methods in Synthetic Biology*, Methods in Molecular Biology, Volume 1244, pages 323-336, 2015.
3. C. Madsen, C. Myers, N. Roehner, C. Winstead, and Z. Zhang, "Efficient Analysis Methods in Synthetic Biology", in *Computational Methods in Synthetic Biology*, Methods in Molecular Biology, Volume 1244, pages 217-257, 2015.
4. A. Fisher, D. Kulkarni, and C. Myers, "A new assertion property language for analog/mixed-signal circuits", in *Languages, Design Methods, and Tools for Electronic System Design - Selected Contributions from FDL 2013*, Lecture Notes in Electrical Engineering, Volume 311, pages 45-65, 2015.
5. C. Myers, "Platforms for Genetic Design Automation", in *Methods in Microbiology 2013: Microbial Synthetic Biology*, November, 2013.
6. C. Myers (editor), *Stochastic Control*, Sciyo, August, 2010.
7. H. Kuwahara, C. Madsen, I. Mura, C. Myers, A. Tejeda, and C. Winstead, "Efficient stochastic simulation to analyze targeted properties of biological systems," in *Stochastic Control*, Sciyo, pages 505-532, August, 2010.
8. H. Kuwahara and C. J. Myers, "Abstraction methods for analysis of gene regulatory networks," in *Computational Methods in Gene Regulatory Networks*, IGI Global, pages 352-385, 2010.
9. E. Brunvand and C. Myers (editors), *2001 Conference on Advanced Research in VLSI*, IEEE Computer Society, March, 2001.
10. T. Suemei, J. Lee, C. Myers, and C. Campbell, "Machine analysis and data coding of the Qing imperial lineage" (in Chinese), in *The Demographic Behavior and Social Environment of the Qing Imperial Lineage*, Beijing University Press, 1994.

Journal Articles

1. H. Baig, P. Fontanarossa, V. Kulkarni, J. McLaughlin, P. Vaidyanathan, B. Bartley, S. Bhakta, S. Bhatia, M. Bissell, K. Clancy, R. Cox, A. Moreno, T. Gorochowski, R. Grunberg, J. Lee, A. Luna, C. Madsen, G. Misirli, T. Nguyen, N. Le Novere, Z. Palchick, M. Pocock, N. Roehner, H. Sauro, J. Scott-Brown, J. Sexton, G.-B. Stan, J. Tabor, L. Terry, M. Vilar, C. Voigt, A. Wipat, D. Zong, Z. Zundel, J. Beal, C. Myers, "Synthetic Biology Open Language Visual (SBOL Visual) Version 2.3", to appear in *Journal of Integrative Bioinformatics*.

2. P. Fontanarrosa, H. Doosthosseini, A. Borujeni, Y. Dorfan, C. Voigt, and C. Myers, "Genetic Circuit Dynamics: Hazard and Glitch Analysis ", in *ACS Synthetic Biology*, 9(9): 2324-2338, September 18, 2020.

3. J. McLaughlin, J. Beal, G. Misirli, R. Grunberg, B. Bartley, J. Scott-Brown, P. Vaidyanathan, P. Fontanarrosa, E. Oberortner, A. Wipat, T. Gorochowski, C. Myers, "The Synthetic Biology Open Language (SBOL) Version 3: Simplified Data Exchange for Bioengineering", in *Frontiers in Bioengineering and Biotechnology*, 8, September 11, 2020.

4. D. Waltemath, M. Golebiewski, M. Blinov, P. Gleeson, H. Hermjakob, M. Hucka, E. Inau, S. Keating, M. Konig, O. Krebs, R. Malik-Sheriff, D. Nickerson, E, Oberortner, H. Sauro, F. Schreiber, L. Smith, M. Stefan, U. Wittig, and C. Myers, "The first 10 years of the international coordination network for standards in systems and synthetic biology (COMBINE)", in *Journal of Integrative Bioinformatics*, 17(2-3), June 1, 2020.

5. F. Schreiber, B. Sommer, T. Czauderna, M. Golebiewski, T. Gorochowski, M. Hucka, S. Keating, M. Konig, C. Myers, D. Nickerson, and D. Waltemath, "Specifications of Standards in Systems and Synthetic Biology: Status and Developments in 2019", in *Journal of Integrative Bioinformatics*, 17(2-3), June 1, 2020.

6. S. Keating, D. Waltemath, M. Konig, F. Zhang, A. Drager, C. Chaouiya, F. Bergmann, A. Finney, C. Gillespie, T. Helikar, S. Hoops, R. Malik-Sheriff, S. Moodie, I. Moraru, C. Myers, A. Naldi, B. Olivier, S. Sahle, J. Schaff, L. Smith, M. Swat, D. Thieffry, L. Watanabe, D. Wilkinson, M. Blinov, K. Begley, J. Faeder, H. Gomez, T. Hamm, Y. Inagaki, W. Liebermeister, A. Lister, D. Lucio, E. Mjolsness, C. Proctor, K. Raman, N. Rodriguez, C. Shaffer, B. Shapiro, J. Stelling, N. Swainston, N. Tanimura, J. Wagner, M. Meier-Schellersheim, H. Sauro, B. Palsson, H. Bolouri, H. Kitano, A. Funahashi, H. Henning, J. Doyle, and M. Hucka, "SBML Level 3: an extensible format for the exchange and reuse of biological models", in *Molecular Systems Biology*, 16(3): e9110, August 1, 2020.

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97. C. J. Myers and T. H.-Y. Meng, "Synthesis of timed asynchronous circuits," in *IEEE Transactions on VLSI Systems*, 1(2): 106-119, June, 1993 (**Invited Paper**).

Patents

1. S. Rotem, P. Beerel, R. Ginosar, R. Kol, C. Myers, K. Stevens, and K. Yun, *Apparatus and method for parallel processing and self-timed marking of variable length instructions*, issued November 2, 1999, number 5,978,899.

2. S. Rotem, P. Beerel, R. Ginosar, R. Kol, C. Myers, K. Stevens, and K. Yun, *Apparatus and method for self-timed marking of variable length instructions having length-affecting prefix bytes*, issued September 7, 1999, number 5,948,096.

3. S. Rotem, P. Beerel, R. Ginosar, R. Kol, C. Myers, K. Stevens, and K. Yun, *Efficient self-timed marking of lengthy variable length instructions*, issued August 24, 1999, number 5,941,982.

4. S. Rotem, P. Beerel, R. Ginosar, R. Kol, C. Myers, K. Stevens, and K. Yun, *Branch instruction handling in a self-timed marking system*, issued August 3, 1999, number 5,931,944.

Refereed Conference and Workshop Papers

1. T. Neupane, C. Myers, C. Madsen, Z. Zhang, and H. Zheng , "STAMINA: STochastic Approximate Model-checker for INfinite-state Analysis", in *Computer Aided Verification, CAV '19*, July, 2019.

2. C. Myers, G. Bader, P. Gleeson, M. Golebiewski, M. Hucka, N. Le Novere, D. Nickerson, F. Schreiber, and D. Waltemath, "A Brief History of COMBINE", in *2017 Winter Simulation Conference*, December, 2017.

3. V. Dubikhin, D. Sokolov, C. Myers, A. Mokhov, and, A. Yakovlev, "Model discovery for analog/mixed-signal circuits", in *2017 Frontiers in Analog CAD Workshop*, July, 2017.

4. V. Dubikhin, C. Myers, D. Sokolov, I. Syranidis, and, A. Yakovlev, "INVITED: Advances in Formal Methods for the Design of Analog/Mixed-Signal Systems", in *2017 Design Automation Conference*, June, 2017.

5. A. Fisher, C. Myers, and P. Li, "Reachability analysis using extremal rates", in 7^{th} *Nasa Formal Methods Symposium*, April, 2015.

6. Z. Zhang, W. Serwe, J. Wu, T. Yoneda, H. Zheng, and C. Myers, "Formal analysis of a fault-tolerant routing algorithm for a network-on-chip", in *19th International Workshop on Formal Methods for Industrial Critical Systems*, September, 2014.

7. A. Fisher, S. Batchu, K. Jones, D. Kulkarni, S. Little, D. Walter, and C. Myers, "LEMA: a tool for the formal verification of digitally-intensive analog/mixed-signal circuits," in *2014 Midwest Symposium on Circuits and Systems*, August, 2014.

8. F. Butzke, C. Myers, M. Moreira, and N. Calazans, "QDI logic for signaling data validity in bundled-data design: a kogge-stone case study," in *2014 International Symposium on Asynchronous Circuits and Systems*, May, 2014.

9. L. Watanabe and C. Myers, "Hierarchical stochastic simulation of genetic circuits," in *2014 Symposium on Theory of Modeling and Simulation*, April, 2014.

10. D. Kulkarni, A. Fisher, and C. Myers, "A new assertion property language for analog/mixed-signal circuits," in *2013 Forum on Design Languages*, September, 2013 (**best paper candidate**).

11. H. Lin, P. Li, and C. Myers, "Verification of digitally-intensive analog circuits via kernel ridge regression and hybrid reachability analysis," in *2013 Design Automation Conference*, June, 2013.

12. N. Miskov-Zivanov, J. Faeder, C. Myers, and H. Sauro, "Modeling and design automation of biological circuits and systems," in *2012 International Conference on Computer-Aided Design*, November, 2012 (**invited**).

13. H. Zheng, A. Price, and C. Myers, "Using decision diagrams to compactly represent state space for explicit model checking," in *2012 IEEE International High Level Design Validation and Test Workshop*, November, 2012.

14. Y. Zhang, E. Rodriguez, H. Zheng, and C. Myers, "An improvement in partial order reduction using behavioral analysis," in *IEEE Computer Society Annual Symp. on VLSI*, August, 2012.

15. H. Zheng, E. Rodriguez, Y. Zhang, and C. Myers, "A compositional minimization approach for large asynchronous design verification," in *19th International SPIN Workshop on Model Checking of Software*, July, 2012.

16. C. Madsen, C. Myers, N. Roehner, C. Winstead, and Z. Zhang, "Utilizing stochastic model checking to analyze genetic circuits," in *2012 Computational Intelligence in Bioinformatics and Computational Biology*, May, 2012 (**best student paper**).

17. D. Kulkarni, S. Batchu, and C. Myers, "Improved model generation of AMS circuits for formal verification," in *2011 Virtual Worldwide Forum for PhD Researchers in Electronic Design Automation*, November, 2011.

18. J. Wu, Z. Zhang, and C. Myers, "A fault-tolerant routing algorithm for a network-on-chip using a link fault model," in *2011 Virtual Worldwide Forum for PhD Researchers in Electronic Design Automation*, November, 2011.

19. H. Kuwahara and C. Myers, "Erlang-delayed stochastic chemical kinetic formalism for efficient analysis of biological systems with non-elementary reaction effects," in *2011 ACM Conference on Bioinformatics, Computational Biology, & Biomedicine*, August, 2011.

20. H. Yao, H. Zheng, and C. Myers, "State space reductions for scalable verification of asynchronous designs," in *2010 IEEE International High Level Design Validation and Test Workshop*, November, 2010.

21. C. Winstead, C. Madsen, and C. Myers, "iSSA: an incremental stochastic simulation algorithm for genetic circuits," in *2010 International Conference on Circuits and Systems*, May, 2010.

22. R. Thacker, K. Jones, C. Myers, and H. Zheng, "Automatic abstraction for verification of cyber-physical systems," in *The 1st ACM/IEEE International Conference on Cyber-Physical Systems*, April, 2010.

23. C. Myers, N. Barker, H. Kuwahara, K. Jones, C. Madsen, and N. Nguyen, "Genetic design automation," in *2009 International Conference on Computer-Aided Design*, November, 2009 (**invited**).

24. R. Thacker, C. Myers, K. Jones, and S. Little, "A new verification method for embedded systems," in *The 27th IEEE International Conference on Computer Design*, October, 2009

25. S. Little and C. Myers, "Abstract modeling and simulation aided verification of analog/mixed-signal circuits," in *Workshop on Formal Verification of Analog Circuits*, July, 2008.

26. N. Nguyen, N. Barker, H. Kuwahara, C. Madsen, and C. Myers, "Synthesis of genetic circuits from graphical specifications," in *2008 International Workshop on Logic Synthesis*, June, 2008 (**Invited**).

27. N. Hamada, Y. Shiga, H. Saito, T. Yoneda, C. Myers, and T. Nanya, "A behavioral synthesis method for asynchronous circuits with bundled-data implementation," in *The 8th International Conference on Application of Concurrency to System Design*, June, 2008.

28. S. Little, A. Sen, and C. Myers, "Application of automated model generation techniques to analog/mixed-signal circuits," in *8th International Workshop on Microprocessor Test and Verification*, December, 2007.

29. S. Little, D. Walter, K. Jones, and C. Myers, "Analog/mixed-signal circuit verification using models generated from simulation traces," in *Automated Technology for Verification and Analysis*, October, 2007.

30. D. Walter, S. Little, and C. Myers, "Bounded model checking of analog and mixed-signal circuits using an SMT solver," in *Automated Tech. for Verif. and Analysis*, October, 2007.

31. F. Beal, T. Yoneda, and C. Myers, "Hazard checking of timed asynchronous circuits revisited," in *7th International Conference on Applications of Concurrency to System Design*, July, 2007.

32. H. Kuwahara and C. Myers, "Production-passage-time approximation: a new approximation method to accelerate the simulation process of enzymatic reactions," in *The Eleventh Annual International Conference on Research in Computational Molecular Biology*, April, 2007.

33. N. Nguyen, H. Kuwahara, C. Myers, and J. Keener, "The design of a genetic Muller C-element," in *The Thirteenth International Symposium on Asynchronous Circuits and Systems*, March, 2007 (**Best Paper Award**).

34. D. Walter, S. Little, N. Seegmiller, C. Myers, and T. Yoneda, "Symbolic model checking of analog/mixed-signal circuits", in *Asia and South Pacific Design Automation Conference 2007*, January, 2007.

35. S. Little, N. Seegmiller, D. Walter, C. Myers, and T. Yoneda, "Verification of analog/mixed-signal circuits using labeled hybrid Petri nets", in *2006 International Conference on Computer-Aided Design*, November, 2006.

36. T. Yoneda and C. Myers, "Effective contraction of timed STGs for decomposition based timed circuit synthesis," in *Automated Technology for Verification and Analysis*, pages 229-244, October, 2006.

37. H. Saito, N. Jindapetch, T. Yoneda, C. Myers, and T. Nanya, "ILP-based scheduling for asynchronous circuits in bundled-data implementation," in *2006 Int. Conf. on Computer and Information Technology*, September, 2006.

38. H. Kuwahara, C. Myers, and M. Samoilov, "Abstracted stochastic analysis of type 1 pili expression in e. coli," in *Proceedings of the 2006 International Conference on Bioinformatics & Computational Biology (BIOCOMP '06)*, pages 125-131, June, 2006.

39. N. Barker, C. Myers, and H. Kuwahara, "Learning genetic regulatory network connectivity from time series data," in *The 19th International Conference on Industrial, Engineering & Other Applications of Applied Intelligent Systems (IEA/AIE'06)*, June, 2006.

40. H. Saito, N. Jindapetch, T. Yoneda, C. Myers, and T. Nanya, "A scheduling method for asynchronous bundled-data implementations based on the completion of data operations," in *2005 Int. Tech. Conf. on Circuits/Systems, Computers and Communication*, July, 2005.

41. H. Saito, N. Jindapetch, T. Yoneda, and C. Myers, "A scheduling method for asynchronous bundled-data implementations," in *2005 Int. Workshop on Logic Synthesis*, June, 2005.

42. H. Kuwahara, C. Myers, N. Barker, M. Samoilov, and A. Arkin, "Asynchronous abstraction methodology for genetic regulatory networks," in *Third International Workshop on Computational Methods in Systems Biology*, April, 2005.

43. C. Myers, R. Harrison, D. Walter, N. Seegmiller, and S. Little, "The case for analog circuit verification," in *Workshop on Formal Verification of Analog Circuits*, April, 2005.

44. T. Yoneda, A. Matsumoto, M. Kato, and C. J. Myers, "High level synthesis of timed asynchronous circuits," in *The Eleventh International Symposium on Asynchronous Circuits and Systems*, pages 210-218, March, 2005.

45. S. Little, D. Walter, N. Seegmiller, C. Myers, and T. Yoneda, "Verification of analog and mixed-signal circuits using timed hybrid Petri nets," in *Automated Technology for Verification and Analysis*, pages 426-440, November, 2004.

46. D. Pradubsuwun, T. Yoneda, and C. Myers, "Partial order reduction for detecting safety and timing failures of timed circuits," in *Automated Technology for Verification and Analysis*, pages 339-353, November, 2004.

47. T. Yoneda, H. Onda, and C. J. Myers, "Synthesis of speed independent circuits based on decomposition," in *The Tenth International Symposium on Asynchronous Circuits and Systems*, pages 135-145, April, 2004.

48. C. Nelson, C. Myers, and T. Yoneda, "Efficient verification of hazard-freedom in gate-level timed asynchronous circuits", in *2003 International Conference on Computer-Aided Design*, pages 424-431, November, 2003.

49. H. Zheng, C. Myers, D. Walter, S. Little, and T. Yoneda, "Verification of timed circuits with failure directed abstractions", in *IEEE International Conference on Computer Design*, pages 28-35, October, 2003.

50. C. Myers, E. Mercer, and H. Jacobson, "Verifying synchronization strategies", in *Formal Methods for Globally Asynchronous Locally Synchronous (GALS) Architecture*, September, 2003 (**Invited paper**).

51. T. Kitai, Y. Oguro, T. Yoneda, E. Mercer, and C. Myers, "Level oriented formal model for asynchronous circuit verification and its efficient analysis method," in *2002 Pacific Rim International Symposium on Dependable Computing*, pages 210-218, November, 2002.

52. T. Yoneda, T. Kitai, and C. Myers, "Automatic derivation of timing constraints by failure analysis," in *Computer Aided Verification, CAV '02*, pages 195-208, July, 2002.

53. C. Winstead, J. Dai, S. Yu, R. Harrison, C. Myers, and C. Schlegel, "Analog decoding of product codes" in *International Symposium on Information Theory*, June, 2002.

54. J. Dai, C. J. Winstead, C. J. Myers, R. R. Harrison, and C. Schlegel, "Cell library for automatic synthesis of analog error control decoders," in *2002 International Conference on Circuits and Systems*, volume 4, pages 481-484, May, 2002.

55. E. Mercer, C. J. Myers, T. Yoneda, and H. Zheng, "Modular synthesis of timed circuits using partial orders on LPNs," in *Theory and Practice of Timed Systems, TPTS '02*, April, 2002.

56. H. Jacobson, P. Kudva, P. Bose, P. Cook, S. Schuster, E. Mercer, and C. J. Myers, "Synchronous interlocked pipelines," in *The Eighth International Symposium on Asynchronous Circuits and Systems*, pages 3-12, April, 2002.

57. B. Zhou, T. Yoneda, and C. Myers "Framework of timed trace theoretic verification revisited," in *The Tenth Asian Test Symposium, ATS '01*, pages 437-442, November, 2001.

58. T. Yoneda, E. Mercer, and C. Myers, "Modular synthesis of timed circuits using partial order reduction" in *The Tenth Workshop on Synthesis and System Integration of MIxed Technologies (SASIMI 2001)*, October, 2001.

59. E. Mercer, C. Myers, and T. Yoneda, "Improved POSET timing analysis in timed Petri nets" in *The Tenth Workshop on Synthesis and System Integration of MIxed Technologies (SASIMI 2001)*, October, 2001.

60. C. Winstead, C. Myers, C. Schlegel, and R. Harrison, "Analog decoding of product codes" in *2001 IEEE Information Theory Workshop*, pages 131-133, September, 2001.

61. H. Zheng, E. Mercer, and C. J. Myers "Automatic abstraction for verification of timed circuits and systems," in *Computer Aided Verification, CAV '01*, pages 182-193, July, 2001.

62. C. Winstead, J. Dai, W. J. Kim, S. Little, Y.-B. Kim, C. Myers, and C. Schlegel, "Analog MAP Decoder for (8,4) Hamming code in subthreshold CMOS" in *2001 IEEE International Symposium on Information Theory*, page 330, June, 2001.

63. K. Killpack, E. Mercer, C. J. Myers, "A standard-cell self-timed multiplier for power and area critical synchronous systems" in *2001 Advanced Research in VLSI Conference*, pages 188-201, March, 2001.

64. C. Winstead, J. Dai, W. J. Kim, S. Little, Y.-B. Kim, C. Myers, and C. Schlegel, "Analog MAP Decoder for (8,4) Hamming code in subthreshold CMOS" in *2001 Advanced Research in VLSI Conference*, pages 132-147, March, 2001.

65. C. J. Myers and H. Jacobson, "Efficient exact two-level hazard-free logic minimization," in *The Seventh International Symposium on Asynchronous Circuits and Systems*, pages 64-73, March, 2001 **(Best Paper Finalist)**.

66. C. J. Myers, W. Belluomini, K. Killpack, E. Mercer, E. Peskin, and H. Zheng, "Timed circuits: a new paradigm for high-speed design", in *Asia and South Pacific Design Automation Conference 2001*, pages 335-340, February, 2001 **(Invited Paper)**.

67. H. Zheng and C. J. Myers, "Automatic abstraction for synthesis and verification of deterministic timed systems" in *2000 ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, December, 2000.

68. H. Jacobson, C. Myers, and G. Gopalakrishnan, "Achieving fast and exact hazard-free logic minimization of extended burst-mode gC finite state machines" in *2000 International Conference on Computer-Aided Design*, pages 303-310, November, 2000.

69. E. Mercer and C. J. Myers, "Stochastic cycle period analysis of timed circuits," in *2000 International Conference on Circuits and Systems*, volume II, pages 172-175, May, 2000.

70. S. T. Jung and C. J. Myers, "Direct synthesis of timed asynchronous circuits," in *1999 International Conference on Computer-Aided Design*, pages 332-337, November, 1999.

71. B. Bachman, H. Zheng, and C. Myers, "Architectural synthesis of timed asynchronous systems", in *IEEE International Conference on Computer Design*, pages 354-363, October, 1999.

72. E. Mercer and C. J. Myers, "Stochastic cycle period analysis of timed circuits," in *1999 International Workshop on Logic Synthesis*, June, 1999.

73. S. T. Jung and C. J. Myers, "Direct synthesis of timed asynchronous circuits," in *1999 International Workshop on Logic Synthesis*, June, 1999.

74. S. Rotem, K. Stevens, R. Ginosar, P. A. Beerel, C. J. Myers, K. Y. Yun, R. Kol, C. Dike, M. Roncken, and B. Agapiev, "RAPPID: An Asynchronous Instruction Length Decoder," in *The Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 60-70, April, 1999 (**Best Paper Award**).

75. W. Belluomini, C. J. Myers, and H. P., Hofstee, "Verification of Delayed-Reset Domino Circuits Using ATACS," in *The Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 3-12, April, 1999.

76. W. Belluomini, C. J. Myers, and H. P., Hofstee, "Verification of Delayed-Reset Domino Circuits Using ATACS," in *1999 ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, March, 1999.

77. R. A. Thacker, W. Belluomini, and C. J. Myers, "Timed circuit synthesis using implicit methods," in *1999 12th VLSI Design Conference*, pages 181-188, January, 1999.

78. W. Belluomini and C. J. Myers "Verification of timed systems using POSETs," in *Computer Aided Verification, CAV '98*, pages 403-415, June, 1998.

79. W. Chou, P. Beerel, R. Ginosar, R. Kol, C. Myers, S. Rotem, K. Stevens, and K. Yun, "Average-case optimized technology mapping of one-hot domino circuits," in *The Fourth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 80-91, April, 1998.

80. W. Belluomini and C. J. Myers, "Timed Event/Level Structures," in *1997 ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, December, 1997.

81. A. E. Sjogren and C. J. Myers, "Interfacing synchronous and asynchronous modules within a high-speed pipeline," in *17th Conf. on Advanced Research in VLSI*, pages 47-61, Sept, 1997.

82. R. A. Thacker and C. J. Myers, "Synthesis of timed circuits using BDDs," in *1997 International Workshop on Logic Synthesis*, May, 1997.

83. C. J. Myers and H. Zheng, "An asynchronous implementations of the MAXLIST algorithm," in *1997 International Conference on Acoustics, Speech, and Signal Processing*, volume 1, pages 647-650, April, 1997.

84. W. Belluomini and C. J. Myers, "Efficient timing analysis algorithms for timed state space exploration," in *The Third International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 88-100, April, 1997.

85. C. J. Myers, P. A. Beerel, and T. H.-Y. Meng, "Technology mapping of timed circuits," in *2nd Working Conference on Asynchronous Design Methodologies*, pages 138-147, June, 1995.

86. C. J. Myers, T. G. Rokicki, and T. H.-Y. Meng, "Automatic synthesis of gate-level timed circuits with choice," in *1995 Chapel Hill Conference on Advanced Research in VLSI*, pages 42-58, March, 1995.

87. T. G. Rokicki and C. J. Myers "Automatic verification of timed circuits," in *Computer Aided Verification, CAV '94*, pages 468-480, June, 1994.

88. C. J. Myers and T. H.-Y. Meng, "Synthesis of timed asynchronous circuits," in *IEEE International Conference on Computer Design, ICCD-1992*, pages 279-284, October, 1992.

Invited Talks

1. DARPA SD2 PI Meeting, Santa Barbara, CA, January 2020
2. Interagency Synthetic Biology Meeting, Washington D.C., October 2019
3. University of Cambridge, Cambridge, United Kingdom, October 2019
4. Shonan, Tokyo, Japan, September 2019
5. COMBINE Forum, Heidelberg, Germany, July 2019
6. Imperial College London, London, United Kingdom, July 2019
7. Oxford Synthetic Biology CDT Symposium, Oxford, United Kingdom, July 2019
8. BioRoboost, Madrid, Spain, June 2019
9. Oxford Global Synthetic Biology Congress, London, United Kingdon, November 2018
10. SB4D Workshop, Arlington, VA, September 2018
11. CMSB 2018, Brno, Czech Republic, September 2018
12. University College London, London, United Kingdom, September 2018
13. NSF Living Computing Project Site Visit, Boston, MA, August 2018
14. SBOL Developers Workshop, Berkeley, CA, July 2018
15. DARPA SD2 PI Meeting, Seattle, WA, July 2018
16. ASYNC 2018, Vienna, Austria, May 2018
17. Dagstuhl Seminar, Germany, March 2018
18. University of Nebraska, Lincoln, NE, October 2017
19. Technical University of Denmark, Copenhagen, Denmark, October 2017
20. SBOL Developers Workshop, Pittsburgh, PA, August 2017
21. SEED Conference, Vancouver, Canada, June 2017
22. Massachusetts Instistute of Technology, Cambridge, MA, May 2017
23. Boston University, Boston, MA, May 2017
24. BBN/Raytheon, Cambridge, MA, April 2017
25. Microsoft Research, Cambridge, UK, March 2017
26. Newcastle University, Newcastle, UK, March 2017
27. University of Oxford, Oxford, UK, March 2017
28. University of Bristol, Bristol, UK, February 2017
29. Imperial College London, London, UK, February 2017
30. SynBioUK 2016, Edinburgh, UK, November 2016
31. University of Oxford, Oxford, UK, November 2016
32. Newcastle University, Newcastle, UK, October 2016
33. COMBINE Workshop, Newcastle, UK, September 2016
34. SBOL Workshop, Newcastle, UK, August 2016
35. HARMONY Workshop, Auckland, New Zealand, June 2016
36. IWBDA, Seattle, WA, August 2015
37. VEMDP Workshop, San Francisco, CA, July 2015
38. Verimag, Grenoble, France, June 2015
39. Inria, Grenoble, France, June 2015
40. HARMONY Workshop, Wittenberg, Germany, April 2015
41. SY-BIO Workshop, Dallas, Texas, March 2015
42. RWTH Aachen, Aachen, Germany, March 2015

43. Whole Cell Summer School, Rostock, Germany, March 2015
44. ICSB Workshop on Standards, Melbourne, Australia, September 2014
45. ICSB Tutorial, Melbourne, Australia, September 2014
46. COMBINE Workshop, Los Angeles, CA, August 2014
47. SEED Conference, Los Angeles, CA, July 2014
48. Inria, Grenoble, France, July 2014
49. HARMONY Workshop, Manchester, UK, April 2014
50. University of California, Davis, CA, January 2014
51. COMBINE Workshop, Paris, France, September 2013
52. International Workshop on Bio-Design Automation, London, UK, July 2013
53. Synthetic Biology 6.0, London, UK, July 2013
54. Design Automation Summer School, Austin, TX, June 2013
55. University of Connecticut Health Science Center, Farmington, CT, May 2013
56. Newcastle University, Newcastle, UK, April 2013
57. University of South Florida, Tampa, CA, April 2013
58. National Tsing Hua University, Hsinchu, Taiwan, March 2013
59. National Taiwan University, Genome and Systems Biology Center, Taipei, Taiwan, March 2013
60. Academia Sinica, Nankang, Taiwan, March 2013
61. National Taiwan University, EECS, Taipei, Taiwan, March 2013
62. Workshop on Design Automation for AMS, San Jose, CA, November 2012
63. ICCAD, San Jose, CA, November 2012
64. COMBINE Workshop, Toronto, Canada, August 2012
65. CAV Tutorial, Berkeley, CA, July 2012
66. RWTH Aachen, Aachen, Germany, May 2012
67. Cornell University, Ithaca, NY, April 2012
68. Intel Corporation, Portland, OR, December 2011
69. COMBINE Workshop, Heidelberg, Germany, September 2011
70. International Conference on Systems Biology Tutorial, Heidelberg, Germany, September 2011
71. Design Automation Summer School, San Diego, CA, June 2011
72. Workshop on Diversity in Design Automation and Test, Pittsburgh, PA, May 2011
73. Dagstuhl Seminar, Germany, April 2011
74. SRC Verification Review, Santa Barbara, CA, April 2011
75. Microsoft Research Cambridge, United Kingdom, October 2010
76. Intel Corporation, Portland, OR, July 2010
77. Dagstuhl Seminar, Germany, July 2010
78. Carnegie Mellon University, Pittsburgh, PA, December 2009
79. Brigham Young University, Provo, UT, November 2009
80. ICCAD Tutorial, San Jose, CA, November 2009
81. CANDE Workshop, Monterey, CA, October 2009
82. Intel Corporation, Portland, OR, October 2009
83. First RoSBNet Synthetic Biology Workshop, Oxford, United Kingdom, September 2009
84. Technical University of Denmark, August 2009
85. Utah State University, Logan, UT, July 2009

86. International Workshop on Bio-Design Automation, San Francisco, CA, July 2009
87. NSF Workshop: EDA-Past, Present, and Future, Washington D.C., July 2009
88. SRC Verification Review, Raleigh, NC, April 2009
89. Caltech, March 2009
90. University of California, Berkeley, October 2008
91. Technical University of Kaiserslautern, Germany, September 2008
92. Dagstuhl Seminar, Germany, September 2008
93. International Conference on Systems Biology Tutorial, Gothenburg, Swedwn, August 2008
94. International Workshop on Logic Synthesis, Lake Tahoe, CA, June 2008
95. IMA Workshop, Minneapolis, MN, April 2008
96. SRC Verification Review, Berkeley, CA, March 2008
97. Banbury Workshop, Cold Spring Harbor, NY, May 2007
98. SRC Verification Review, Salt Lake City, UT, April 2007
99. University of California, Berkeley, CA, March 2007
100. Cadence Berkeley Labs, Berkeley, CA, March 2007
101. EPFL, Laussane, Switzerland, June 2006
102. NSF/ECS Grantees Workship, Tuskegee, AL, June 2006
103. University of Southern California, May 2006
104. SRC Verification Review, Pittsburgh, PA, April 2006
105. David Evans Conference on CE, Heber City, UT, May 2005
106. Caltech, May 2005
107. SRC Verification Review, Boulder, CO, March 2005
108. Southern Taiwan University of Technology, Tainan, Taiwan, November 2004
109. Brigham Young University, November 2004
110. Kitano Symbiotic Systems Group, Tokyo, June 2004
111. SRC Verification Review, Princeton, NJ, March 2004
112. BioMath Seminar, U. of Utah, December 2003
113. Bioengineering Seminar, U. of Utah, September 2003
114. FMGALS 2003, September 2003
115. Human Genome Center, U. of Tokyo, May 2003
116. Research Center for Advanced Science and Technology, U. of Tokyo, May 2003
117. SRC Verification Review, Austin, TX, April 2003
118. UC Berkeley, February 2003
119. Stanford University, February 2003
120. David Evans Conference on CE, Heber City, UT, June 2002
121. SRC Verification Review, Salt Lake City, UT, March 2002
122. SRC Verification Review, Pittsburgh, PA, March 2001
123. ASP-DAC 2001, February 2001
124. Lucent Technologies, November 2000
125. Sonic Innovations, September 2000
126. SUN Microsystems, June 2000
127. SRC Verification Review, Austin, TX, March 2000
128. Caltech, March 2000

129. Asynchronous design tutorial for Samsung, July 1999
130. SRC CAD Review, Irvine, CA, March 1999
131. ASYNC98, CAD demo, San Diego, CA, April 1998
132. SRC CAD Review, Austin, TX, March 1998
133. IBM Austin Research Laboratory, June 1997
134. Stanford University, May 1997
135. Technical University of Denmark, April 1997
136. University of Manchester, April 1997
137. ASYNC97, CAD demo, Eindhoven, Netherlands, April 1997
138. Intel Portland, August 1996
139. Caltech, May 1996
140. 3-day short course on asynchronous design, Intel Portland, April 1996
141. ASYNC96, CAD demo, Aizu, Japan, March 1996
142. Beijing Institute of Machinery, March 1996
143. Intel Portland, September 1995
144. Intel Israel, August 1995
145. Phillips Nat Lab in Eindhoven, Netherlands, June 1995
146. IMEC in Leuven, Belgium, June 1995
147. University of Manchester, June 1995
148. SUN Microsystems, April 1995