

Curriculum Vitae, Ganesh Lalitha Gopalakrishnan
School of Computing, University of Utah, Salt Lake City, UT 84112-9205
(801) 581-3568 (Fax 5843) – ganesh@cs.utah.edu – <http://www.cs.utah.edu/~ganesh>

EDUCATION

- Ph.D. in Computer Science, State University of New York at Stony Brook, NY, Dec. 1986.
Dissertation title: “From Algebraic Specifications to Correct VLSI Systems.”
Advisors: Profs. D. R. Smith and M. K. Srivas.
- M.Tech. Elec. Engg., Indian Institute of Technology, Kanpur, India, 1980.
- B.Sc. Elec. Engg., National Institute of Technology (former REC) Calicut, India, 1978.

EMPLOYMENT

- August 2016 to July 2017: Sabbatical Activity: (1) Finishing my 2019 book “Automata and Computability: A Programmer’s Perspective”; (2) Research on System Resilience and Reproducibility (in collaboration with the Pacific Northwest National Laboratory and the Lawrence Livermore National Laboratory).
- July 2009 to June 2010: Sabbatical Activity: Concurrency Curriculum Development with the RiSE group, Microsoft Research, Redmond, WA.
- **July 2000 to present: Professor**, School of Computing, University of Utah, Salt Lake City, UT.
- August 2002 to June 2003: Sabbatical Activity: Post-Silicon Verification, Intel Corporation, Santa Clara, CA.
- **July 1993 to June 2000: Associate Professor**, Computer Science, University of Utah, Salt Lake City, UT.
- September 1995 to May 1996: Sabbatical Activity: Formal Verification, Dill group, Stanford University.
- August 1988 to July 1989: Visiting Assistant Professor, Birtwistle group, Computer Science, University of Calgary.
- **September 1986 to June 1993: Assistant Professor**, Computer Science, University of Utah.
- August 1980 to July 1981: Research Associate, Rajaraman group, Department of Computer Science, Indian Institute of Technology, Kanpur, India.

CAREER HIGHLIGHTS, AWARDS, INVITED TALKS

- Career Highlights
 - 2017: PI from Utah of the “PRUNERS” project that was Finalist in the R&D 100 selection (collaboration with LLNL and RWTH Aachen)
 - 2015: Senior Member, IEEE
 - 2014: ACM Distinguished Scientist
 - 2012: Beacons of Excellence Award, Student Affairs, Utah. Award Citation:https://archive.unews.utah.edu/news_releases/u-announces-new-beacons-of-excellence-award/
- Students, Leadership, Editorship
 - Primary advisor of 25 PhD students (defended) and 4 current PhD students. Full list on Page 6.
 - Undergraduate REU Mentoring: 51 students over career (full list on Page 8)
 - 2009: Director, Center for Parallel Computing at Utah (<http://www.parallel.utah.edu>).
 - 1999 onwards: Associate Editor, Journal of Formal Methods in System Design (Springer).
- 2018: One-week Course, Oct 8-13 on “High Performance Computing Concepts and Practice”

at NIT, Calicut, as part of the Global Initiative of Academic Networks (GIAN) program. <http://http://www.nitc.ac.in/GIAN/HPCCP/>.

- ACM Distinguished Speaker (appointed 2019). Talks given to date:
 - 2022: Sonoma State University, CA, “System Resilience: Amplify Failures, Detect, or Both?” (virtual talk), part of the ACM Distinguished Speakers Program.
 - 2019: BYU Rexburg, ID, October 10, “Automata and Computability using Jupyter and Formal Methods.”
 - 2019: Boise State University, Boise, ID, October 8, “Keeping Science on Keel when Software Moves.”
 - 2019: Montana State University, Bozeman, MT, October 7, “Keeping Science on Keel when Software Moves.”
- INVITED TALKS (2019-2020):
 - 2020: “Symbolic AD with conditionals for error and instability analysis,” Workshop on Program Synthesis for Scientific Computing, Argonne (on Zoom). <https://prog-synth-science.github.io/2020/#agenda>
 - 2020: “The Grass is Really Green on the Other Side: Empirical vs. Rigorous in Floating-Point Precision Analysis, Reproducibility, Resilience,” ICERN Workshop on Variable Precision in Mathematical and Scientific Computing, May 7 - 8, 2020 (on Zoom). URL: <https://icerm.brown.edu/events/htw-20-vp/>
 - 2019: Keynote in CnC Workshop, December 3, “How to Sugarcoat System Resilience?”
 - 2019: Invited Talk at Argonne National Laboratory, July 29, 2019, “Keeping Science on Keel When Software Errs or Moves.ap”
 - 2019: Invited Talk in the ROSS 2019 workshop, June 25, “System Resilience: Amplify Failures, Detect, or Both?”

RESEARCH AND FUNDING (2019-2021)

- 2021: PI, ComPort: Rigorous Testing Methods to Safeguard Software Porting (part of the DOE/ASCR X-Stack Award for \$3.4 million with six total senior investigators). News Story at <https://www.coe.utah.edu/2021/09/24/soc-faculty-receive-doe-ascr-x-stack-award/>.
Details of the Utah Award:
 - Role: Ganesh Gopalakrishnan is PI and Project Lead
(Pavel Panchekha is Co-PI)
 - Sponsor: Department of Energy
 - Total Award Amount: \$750,000
 - Location of Project: University of Utah
 - Effort: 1 summer month
 - Period: 09/1/2021 to 08/31/2024
- 2021: PI, Collaborative Research: FMitF: Track-1: Correctness at Both Ends (CBE): Rigorous ML Meets Correct and Efficient Sparse Implementations
 - Role: PI (Aditya Bhaskara is Co-PI, with equal budget split)
 - Sponsor: National Science Foundation
 - Total Award Amount: \$450,000
 - Location of Project: University of Utah
 - Effort: 0.5 summer month
 - Period: 09/1/2021 to 08/31/2024

- 2020: PI, *Collaborative Research: SHF: Medium: Practical and Rigorous Correctness Checking and Correctness Preservation for Irregular Parallel Programs*, \$447,570, August 2020 through July 2023. (Collaboration with University of Delaware and Texas State University.)
- 2019: PI, *FMTF: Track II: Rigorous and Versatile Float-Point Precision Analysis and Tuning*, \$100,000 awarded Apr 2019 - Dec 2021.

BOOKS

1. 2019: **Undergraduate textbook.** Ganesh Lalitha Gopalakrishnan, “Automata and Computability: A Programmer’s Perspective” (328 pages). CRC Press. ISBN 978-1-138-55242-5.
2. **Undergraduate textbook.** Ganesh Lalitha Gopalakrishnan, “Computation Engineering: applied automata theory and logic” (505 pages). Springer, ISBN 0-387-24418-2, 2006.
3. Ganesh Gopalakrishnan and Shaz Qadeer, editors. Proceedings of the 23rd International Conference on Computer Aided Verification (CAV), Snowbird, UT, July 2011. LNCS 6806.
4. Konrad Slind, Annette Bunker, and Ganesh Gopalakrishnan (Eds.), Theorem Proving in Higher Order Logics, 17th International Conference, TPHOLS 2004, Park City, Utah, USA, September 14-17, 2004, Lecture Notes in Computer Science, Vol. 3223. ISBN: 3-540-23017-3
5. Ganesh Gopalakrishnan and Phillip Windley, editors. Formal Methods in Computer-Aided Design. Proceedings of the 2nd International Conference, FMCAD ’98. Lecture Notes in Computer Science 1522, Springer-Verlag, 1998, 538 pages. ISSN 0302-9743.

PAPERS DURING 2017-2021 (For full list, please see Page 22.)

1. 2021:
 - (a) Ganesh Gopalakrishnan, Ignacio Laguna, Ang Li, Pavel Panchekha, Cindy Rubio-Gonzalez, and Zachary Tatlock, “The Unfledged State of Heterogeneous System Testing,” Workshop on the Science of Scientific-Software Development and Use, <https://web.cvent.com/event/1b7d7c3a-e9b4-409d-ae2b-284779cfe72f/summary>, December 2021.
 - (b) Ganesh Gopalakrishnan, Ignacio Laguna, Ang Li, Pavel Panchekha, Cindy Rubio-Gonzalez and Zachary Tatlock, “Guarding Numerics Amidst Rising Heterogeneity,” Correctness 2021: Fifth International Workshop on Software Correctness for HPC Applications (an SC’21 workshop).
 - (c) Saeed Taheri and Ganesh Gopalakrishnan, “GoAT: Automated Concurrency Analysis and Debugging Tool for Go,” 2021 IEEE International Symposium on Workload Characterization.
 - (d) Arnab Das, Tanmay Tirpankar, Ganesh Gopalakrishnan, Sriram Krishnamoorthy, “Robustness Analysis of Loop-Free Floating-Point Programs via Symbolic Automatic Differentiation,” IEEE Cluster, 2021.
 - (e) Dong H. Ahn, Allison H. Baker, Michael Bentley, Ian Briggs, Ganesh Gopalakrishnan, Dorit M. Hammerling, Ignacio Laguna, Gregory L. Lee, Daniel J. Milroy, and Mariana Vertenstein, “Keeping science on keel when software moves,” Commun. ACM 64(2): 66-74 (2021).
2. 2020:
 - (a) Vinu Joseph, Shoaib Ahmed Siddiqui, Aditya Bhaskara, Ganesh Gopalakrishnan, Saurav Muralidharan, Michael Garland, Sheraz Ahmed, and Andreas Dengel, “Reliable Model Compression via Label-Preservation-Aware Loss Functions,” arXiv 2012.01604.
 - (b) Vinu Joseph, Saurav Muralidharan, Animesh Garg, Michael Garland, and Ganesh L. Gopalakrishnan, “A Programmable Approach to Neural Network Compression,” IEEE Micro, Special Issue on ML for Systems (Track 2), Sept/Oct 2020.
 - (c) Arnab Das, Ian Briggs, Ganesh Gopalakrishnan, Pavel Panchekha, and Sriram Krishnamoorthy, “Scalable yet rigorous floating-point error analysis,” Supercomputing 2020.

Arnab Das won the Best Student Paper of SC'20.

- (d) Arnab Das, Sriram Krishnamoorthy, Ian Briggs, Ganesh Gopalakrishnan, and Ramakrishna Tipireddy, “FPDetect: Efficient Reasoning About Stencil Programs Using Selective Direct Evaluation,” *ACM Transactions on Architecture and Code Optimization (TACO)*, Article 19, Volume 17, Number 3, <https://doi.org/10.1145/3402451>, August 2020.
 - (e) Samuel Thayer, Ganesh L. Gopalakrishnan, Ian Briggs, Michael Bentley, Dong H. Ahn, Ignacio Laguna, and Gregory L. Lee, “POSTER: ArcherGear: Data Race Equivalencing for Expeditious HPC Debugging,” *PPoPP 2020 Poster Paper*, February 2020.
3. 2019:
- (a) Kento Sato, Ignacio Laguna, Gregory L. Lee, Martin Schulz, Christopher M. Chembreau, Simone Atzeni, Michael Bentley, Ganesh Gopalakrishnan, Zvonimir Rakamaric, Geof Sawaya, Joachim Protze, and Dong H. Ahn. “PRUNERS: Providing reproducibility for uncovering non-deterministic errors in runs on supercomputers,” *The International Journal of High Performance Computing Applications*. 33 (5), 2019. <https://doi.org/10.1177/1094342019834621>.
 - (b) Vinu Joseph, Saurav Muralidharan, Animesh Garg, Michael Garland, and Ganesh Gopalakrishnan, “A Programmable Approach to Model Compression,” <https://arxiv.org/abs/1911.02497>.
 - (c) VanderMerwe, Mark, Vinu Joseph, and Ganesh Gopalakrishnan, “Message Scheduling for Performant, Many-Core Belief Propagation,” *IEEE High Performance Extreme Computing Conference (HPEC)*, 2019. (Student best-paper finalist.)
 - (d) Taheri, Saeed, Ian Briggs, Martin Burtscher, and Ganesh Gopalakrishnan, “DiffTrace: Efficient Whole-Program Trace Analysis and Diffing for Debugging,” *IEEE Cluster*, 2019.
 - (e) Ian Briggs, Arnab Das, Vishal Sharma, Mark Baranowski, Sriram Krishnamoorthy, Zvonimir Rakamaric, and Ganesh Gopalakrishnan, “FailAmp: Relativization Transformation for Soft Error Detection in Structured Address Generation.” *ACM Transactions on Architecture and Code Optimization (TACO)* December 2019 Article No.: 50. <https://doi.org/10.1145/3369381>
 - (f) Michael Bentley, Ian Briggs, Ganesh Gopalakrishnan, Dong H. Ahn, Ignacio Laguna, Gregory L. Lee, and Holger E. Jones, *Multi-level analysis of compiler-induced variability and performance tradeoffs*, The 28th International Symposium on High-Performance Parallel and Distributed Computing (HPDC) conference, Phoenix, AZ, June 2019.
4. 2018:
- (a) Alexey Solovyev, Marek S. Baranowski, Ian Briggs, Charles Jacobsen, Zvonimir Rakamaric, and Ganesh Gopalakrishnan, *Rigorous Estimation of Floating-Point Round-off Errors with Symbolic Taylor Expansions*. *ACM Trans. Program. Lang. Syst.* 41, no. 1 (December 2018): 2:1–2:39. doi:10.1145/3230733.
 - (b) Saeed Taheri, Sindhu Devale, Martin Burtscher, and Ganesh Gopalakrishnan. *ParLoT: Efficient Whole-Program Call Tracing for HPC Applications*. *Extreme-Scale Programming Tools Workshop (ESPT) at SC'18*, November 2018.
 - (c) Simone Atzeni, Ganesh Gopalakrishnan, Zvonimir Rakamaric, Ignacio Laguna, Gregory L. Lee, and Dong H. Ahn, “Sword: A Bounded Memory-Overhead Detector of OpenMP Data Races in Production Runs,” *IPDPS*, May, Vancouver, 2018. (Won the LLNL Deputy Director’s S&T Excellent Publication Award.)
 - (d) Simone Atzeni and Ganesh Gopalakrishnan, “An Operational Semantic Basis for Building an OpenMP Data Race Checker,” *HIPS Workshop (part of IPDPS)*, May, Vancouver.
5. 2017:
- (a) Ganesh Gopalakrishnan, Paul D. Hovland, Costin Iancu, Sriram Krishnamoorthy, Ignacio Laguna, Richard A. Lethin, Koushik Sen, Stephen F. Siegel, and Armando Solar-

Lezama, “Report of the HPC Correctness Summit,” 2017. <https://arxiv.org/abs/1705.07478>.

- (b) K. Sato, I. Laguna, G. Lee, M. Schulz, C. Ch�ambreau, D. Ahn, S. Atzeni, M. Bentley, G. Gopalakrishnan, Z. Rakamaric, G. Sawaya, J. Protze (LLNL, Univ. of Utah, RWTH Aachen Univ.), “PRUNERS: Providing Reproducibility for Uncovering Non-Deterministic Errors in Runs on Supercomputers,” CRE 2017 workshop.
- (c) G. Sawaya, M. Bentley, I. Briggs, G. Gopalakrishnan, and D. Ahn, *FLiT: Cross-Platform Floating-Point Result-Consistency Tester and Workload*, IEEE International Symposium on Workload Characterization, October 2017.
- (d) Wei-Fan Chiang, Mark Baranowski, Ian Briggs, Alexey Solovyev, Ganesh Gopalakrishnan, and Zvonimir Rakamaric, *Rigorous floating-point mixed-precision tuning*, POPL 2017: 300-315.

CONFERENCE TUTORIALS (2019-2020) (For prior list, see Page 12.)

1. Ganesh Gopalakrishnan, Ang Li, Pavel Panchekha, Cindy Rubio-Gonzalez, and Zachary Tatlock, “Testing Numerical Code for Heterogeneity: Lessons Learned and Emerging Projects,” MS44, Virtual Conference: 2022 SIAM Conference on Parallel Processing for Scientific Computing, Organizer: Ignacio Laguna, Lawrence Livermore National Laboratory, February 2022.
2. (Half-day Tutorial) Ignacio Laguna (organizer), Michael Bentley, Ian Briggs, and Ganesh Gopalakrishnan, Tutorial on Floating-Point Analysis and Reproducibility Tools for Scientific Software, Los Alamos National Laboratory, January 2020.
3. (Full-day Tutorial) Ignacio Laguna (organizer), Michael Bentley, Ian Briggs, Ganesh Gopalakrishnan, Hui Guo, Michael O. Lam, Harshitha Menon, Pavel Panchekha, and Cindy Rubio Gonzalez, “Tutorial on Floating-Point Analysis and Reproducibility Tools for Scientific Software,” Supercomputing (SC’19), Denver, CO, Nov 17th, 2019.
4. (Half-day Tutorial) Ignacio Laguna (organizer) Michael Bentley, Ian Briggs, Ganesh Gopalakrishnan, Harshitha Menon, Cindy Rubio Gonzalez, Tristan Lucas Vanderbruggen, “Tutorial on Floating-Point Analysis Tools,” Practice and Experience in Advanced Research Computing (PEARC19), Chicago, IL, Jul 30th, 2019.

RECENT SOFTWARE RELEASES (3 Years) (For prior list, see Page 9.)

1. 2020: Software item: **Satire**: Software behind our SC’20 paper “Scalable yet rigorous floating-point error analysis.” <https://github.com/arnabd88/Satire>. Author: Arnab Das (with help from Ian Briggs and Tanmay Tirpankar).
2. 2019: Software item: **FLiT**: Authors: Michael Bentley and Ian Briggs. <https://github.com/PRUNERS/FLiT> *Floating-point Litmus Tests (FLiT) is a C++ test infrastructure for detecting variability in floating-point code caused by variations in compiler code generation, hardware and execution environments. It is used within LLNL.*
3. 2018: Archer OpenMP Race Detector. Archer was part of the PRUNERS tool suite that was a 2017 R&D 100 Award Finalist. It is the only one upstreamed to LLVM, and part of the next LLVM release after version 9.0. <https://github.com/PRUNERS/Archer>
4. 2018: **Jove**: Author: Ganesh Gopalakrishnan. In support of “Automata and Computability using Jupyter,” written for textbook “Automata and Computability: Programmer’s Perspective.” <https://github.com/ganeshutah/Jove.git>.

SELECTED STUDENT ACCOMPLISHMENTS

1. Test-of-time Honorable Mention (Awarded in 2020, for paper authored in 2010): Foundations of Software Engineering. Ph.D. Student: Guodong Li. Paper citation: Guodong Li and Ganesh Gopalakrishnan, “Scalable SMT-based verification of GPU kernel functions.”
2. Best Student Paper (Awarded in 2020), Supercomputing (SC) 2020; Ph.D. Student: Arnab

- Das. Paper citation: Arnab Das, Ian Briggs, Sriram Krishnamoorthy, and Pavel Panchekha, “Scalable yet Rigorous Floating-Point Error Analysis.”
3. Lawrence Livermore National Laboratory Director’s 2020 Excellence in Publication (Student Category Winner). Ph.D. Student: Michael Bentley. Paper citation: Michael Bentley, Ian Briggs, Ganesh Gopalakrishnan, Dong H. Ahn, Ignacio Laguna, Gregory L. Lee, Holger E. Jones, “Multi-Level Analysis of Compiler-Induced Variability and Performance Tradeoffs.”
 4. 2019: Vinu Joseph (PhD Student of self), Winner, NVIDIA Graduate Fellowship for 2020-2021. (One of the 5 winners out of 330 applicants.)
 5. 2019: Mark Van der Merwe (UG of self): Best Paper Finalist (HPEC’19); Outstanding CRA undergraduate honorable mention in 2019; Intern, MILA (Quebec Artificial Intelligence Institute), Montreal.
 6. 2013: Tyler Sorensen (UG of self) was one of the finalists of the CRA Outstanding Undergraduate Researcher selection of 2013.
 7. 2013: Wei-Fan Chiang (PhD student co-advised with Zvonimir Rakamarić), Winner, NVIDIA Graduate Fellowship, 2013-2014.
 8. 2012: Peng Li (PhD Student of self), NVIDIA Graduate Fellowship Winner of 2012-2013.
 9. 2012: Grant Ayers (UG of self), Outstanding CRA undergraduate honorable mention in 2012.
 10. 2009: Michael Delisi (UG of self), one of the finalists of the CRA Outstanding Undergraduate Researcher selection of 2009.

CURRENT Ph.D. STUDENTS

1. Xinyi Li (Est. defense in 2023)
2. Tanmay Tirpankar (Est. defense in 2024)
3. John Jacobson (Est. defense in 2024)
4. Tripti Agarwal (Est. defense in 2024)

GRADUATED Ph.D. STUDENTS (coadvisorships noted; else main advisor)

25. 2021, Saeed Taheri (Miso Robotics)
24. 2021, Vinu Joseph (Nvidia Research Labs)
23. 2021, Mohammed S. Al-Mahfoudh (I was co-advisor; Advisor was Prof. Ryan Stutsman)
22. 2020, Arnab Das, (Apple)
21. 2017, Simone Atzeni (Nvidia)
20. 2016, Wei-Fan Chiang (Software Engineer JP Morgan)
19. 2016, Vishal Sharma (Microsoft)
18. 2016, Sriram Aananthakrishnan (Intel)
17. 2015, Peng Li (Byte-Dance)
16. 2012, Subodh Sharma (Assistant Professor, Computer Science, IIT Delhi)
15. 2011, Anh Vo (Microsoft)
14. 2010, Sarvani Vakkalanka (Google)

13. 2010, Guodong Li (Google)
12. 2009, Yu Yang (Pinterest)
11. 2008, Xiaofang Chen (Pinterest)
10. 2007, Robert Palmer (Tableau Software)
9. 2006, Ritwik Bhattacharya (Microsoft)
8. 2004, Ali Sezgin (Aselan)
7. 2004, Yue Yang (Amazon)
6. 2003, Annette Bunker (I was co-advisor; Advisor was Konrad Slind) Intel
5. 2001, Mike Jones (Associate Professor, Brigham Young University)
4. 2000, Ravi Hosabettu (Juniper Networks)
3. 1999, Ratan Nalumasu (Google)
2. 1996, Prabhakar Kudva (Research Staff Member, IBM)
1. 1992, Venkatesh Akella (Professor, ECE, UC Davis)

CONFERENCE, WORKSHOP ORGANIZATION

- 2017: Principal Investigator and primary organizer, 2017 NSF SI2 PI Meeting, February 21-22, Arlington, VA. <https://nsf-si2-pi.figshare.com/>
- 2016: Area Vice Chair (Chair was Prof. Michelle Strout), Programming Languages Track, Supercomputing Conference, Salt Lake City.
- 2012: Co-Organizers Sebastian Burkhart, Azadeh Farzan, Ganesh Gopalakrishnan, Stephen Siegel, Helmut Veith, and Josef Widder, “Exploiting Concurrency Efficiently and Correctly – (EC)²,” CAV 2012 Workshop, July 7-13, 2012, Berkeley, CA
- 2011: Co-General-Chair (with Shaz Qadeer) Computer Aided Verification (CAV), Snowbird, UT, July 2011.
- 2011: Co-Organizers Sebastian Burkhart, Swarat Chaudhuri, Azadeh Farzan, Ganesh Gopalakrishnan, Stephen Siegel, and Helmut Veith, “Exploiting Concurrency Efficiently and Correctly – (EC)²,” CAV 2011 Workshop, July 14-15, 2011, Snowbird, UT
- 2010: Co-Organizers Rajeev Alur, Swarat Chaudhuri, Azadeh Farzan, Ganesh Gopalakrishnan, Stephen Siegel, and Helmut Veith, “Exploiting Concurrency Efficiently and Correctly – (EC)²,” CAV 2010 Workshop, July 20-21, 2010, Edinburgh, Scotland,
- 2009: General Chair, PADTAD 2009, Chicago, Illinois, USA, July 19-20, ACM 2009. (Ganesh Gopalakrishnan, Eitan Farchi, and Eric Mercer: Proceedings of the 7th Workshop on Parallel and Distributed Systems: Testing, Analysis, and Debugging.
- 2009: Co-Organizers Rajeev Alur, Ganesh Gopalakrishnan, Vineet Kahlon, Madhusudan Parthasarathy, Stephen Siegel, and Helmut Veith, “Exploiting Concurrency Efficiently and Correctly – (EC)²,” CAV 2009 Workshop, June 26-27, 2009, Grenoble, France.
- 2008: Co-Organizers Rajeev Alur, Ganesh Gopalakrishnan, Vineet Kahlon, and Stephen Siegel, “Exploiting Concurrency Efficiently and Correctly – (EC)²,” CAV 2008 Workshop, July 7-8, 2008, Princeton, NJ.

- 2007: *Volume 193, Pages 1-80 (1 November 2007)*, Edited by G. Gopalakrishnan, “Festschrift honoring Gary Lindstrom on his retirement from the University of Utah after 30 years of service,” Salt Lake City, UT, USA 05 May 2007, *Electronic Notes in Theoretical Computer Science (ENTCS)*.
- 2006: Principal Organizer (co-organizer is John O’Leary of Intel), “Multithreading in Hardware and Software: Formal Approaches to Design and Verification (TV’06),” Seattle, August 20-21, 2006 (a post-CAV 2006 workshop). Preface, *Electr. Notes Theor. Comput. Sci.* 174(9): 1-4 (2007).
- 2006: Workshop Chair, Post FMCAD 2006 workshop, Nov 2006, “Post-Silicon Verification and Property Driven Testing.”
- 2000: General Chair, “Tutorial and Workshop on Formal Specification and Verification Methods for Shared Memory Systems (MPV),” Austin, TX, October 31, 2000.
- 2000: General Chair, Workshop on Advances in Verification (WAVE), Chicago, IL, July 20, 2000 (Post CAV’2000 workshop).
- 1998: Co-General-Chair (with Phillip Windley), Internal Symposium on Formal Methods in Computer-Aided Design (FMCAD), November 1998.
- 1998: Member, Organizing Committee of the 21st Century Engineering Consortium Workshop on Formal Methods Education, Sponsored by Rome Labs, DARPA. Melbourne, Florida, March, 1998.
- 1994: Founding Co-chair, “Symposium on Advanced Research on Asynchronous Circuits and Systems,” Salt Lake City, UT, November 3-5, 1994.
- 1993: Co-organizer (with Erik Brunvand) a 1.5-day “mini-track” on self-timed systems as part of the 26th Hawaiian International Conference on Systems Sciences (HICSS), January, 1993.

UNDERGRADUATE REUs MENTORED

1. Omid Saadati
2. Robert Palmer
3. Tyler Sorensen
4. Brandon Gibson
5. Bruce Bolick
6. Kevin Bolick
7. Charlie Jacobsen
8. Trudy Firestone (F)
9. Tony Tuttle
10. Jason Williams
11. Geof Sawaya
12. Sam Larson
13. Mark Stephenson
14. Michael DeLisi
15. Michael Bentley
16. Alan Humphrey
17. Chris Derrick
18. Sergio Rodriguez
19. Wesley Larson
20. Zepeng Zhao
21. Leif Anderson
22. Kevin Avery
23. Grant Ayers

24. Richard Sharp
25. Ben Prather
26. Jacob Tripp
27. Eun Yong Kang
28. Steve Barrus
29. Mark Baranowski
30. Courtney Taylor Burness (F)
31. Sam Zachary
32. Heath French
33. Jamie Hall (F)
34. Mark van der Merwe
35. Sam Thayer
36. Carlos Jiminez
37. Austin Watkins
38. Paul Carlson
39. John Jacobson
40. Keaton Rowley (F)
41. Nithin Chalapathi (UROP winner, 2020)
42. Emil Geisler (UROP winner, 2020-21)
43. Sahana Kargi (UROP winner, 2021)
44. Carson Storm (UROP winner, 2021)
45. Marissa Angell (F)
46. Eric O'Donoghue
47. Andrew Osterhout
48. Aishwarya Athani (F)
49. Eric Sims
50. Ishaan Rajan
51. Cayden Lund

OLDER SOFTWARE RELEASES

1. Software item: **VULFI**: Vishal C. Sharma. Release of Presage, Vector oriented Utah LLVM Fault Injector (VULFI), jointly developed with PNNL. <https://github.com/utahfmr/VULFI>, 2017.
2. Software item: **S3FP: S3FP, a search based floating-point precision analysis framework**. AUTHOR: Wei-Fan Chiang (PhD student). Release at <https://github.com/soarlab/S3FP>.
3. Software item: **GKLEE**: AUTHORS: Peng Li, Guodong Li, and Geof Sawaya. Release at <http://www.cs.utah.edu/fv/GKLEE>, 2013.
4. **GEM, a Graphical Explorer of MPI Programs**. AUTHOR: Alan Humphrey and Chris Derrick. Release at <http://www.cs.utah.edu/fv/GEM> in 2010. GEM has been mentioned in the New and Noteworthy section of Eclipse Parallel Tools Platform (PTP) http://wiki.eclipse.org/PTP/new_and_noteworthy/3.0.0.
5. **Prover of User GPU Programs (PUG)**. AUTHOR: Guodong Li. Release at <http://www.cs.utah.edu/fv/PUG> in 2010.
6. **ISP, a dynamic formal verification tool for MPI programs**. AUTHORS: Sarvani Vakkalanka, Anh Vo and Michael DeLisi. Release at <http://www.cs.utah.edu/fv/ISP>, in 2009.
7. **Inspect, dynamic formal verification of shared memory thread programs**. AUTHOR: Yu Yang. Release at <http://www.cs.utah.edu/fv/Inspect>, in 2009.

8. **Eddy Murphi, a distributed (via MPI) Murphi model checker.** AUTHOR: Igor Melatti. Release at <http://www.cs.utah.edu/fv/EddyMurphi>, in 2007.

PROFESSIONAL ACTIVITIES

2022

- Member of Program Committee, ASPLOS 2023 (Architecture Support for Programming Languages and Operating Systems)
- Member of Program Committee, Supercomputing (SC) 2022, in the track *Programming Frameworks and System Software*
- 2021: November External PhD Examiner, Perpignan University, France.
- 2018: February, External PhD Examiner, Twente University, Twente, The Netherlands.
- Reviewer, ECOOP Journal (4 papers)
- Reviewer, IEEE Transactions on Software Engineering (2 papers)
- Reviewer, Journal of Logical and Algebraic Methods in Programming
- Tutorials committee, International Supercomputing Conference.

During 2017

- External Review Committee (ERC) Member, Architectural Support for Programming Languages and Operating Systems (ASPLOS).
- External Review Committee (ERC) Member, Architectural Support for Programming Languages and Operating Systems (ASPLOS).

During 2016

- External Review Committee (ERC) Member, Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2016, Atlanta, Georgia, April 2-6, 2016.

Prior to 2016

- Program Committee, EuroMPI, 2015.
- External Review Committee (ERC) Member, Micro 2015 (The 48th Annual IEEE/ACM International Symposium on Microarchitecture).
- SC15 BoF on “Reproducibility of High Performance Codes and Simulations – Tools, Techniques, Debugging,” Birds of a Feather at Supercomputing 2015. <https://gcl.cis.udel.edu/sc15bof.php>.
- PC Member (ERC), Progr. Lang. Design and Implementation (PLDI), 2015.
- PC Member (ERC), Architectural Support for Programming Languages and Systems (ASPLOS), 2015.

2014

- PC Member, Princ. and Pract. of Parallel Programming (PPoPP), Orlando, Florida, 2014.
- PC Member, Progr. Lang. Design and Implementation (PLDI), Edinburgh, UK, 2014.
- PC Member, 14th Intl. Conf. on Runtime Verification, September 2014, Toronto, Canada.
- PC Member, EuroMPI/ASIA 2014, Kyoto, Japan, 9-12 September, 2014.

2013

- PC member, Intl. Supercomputing Conference 2013 (Tutorials)
- PC member, Supercomputing (SC) 2013
- PC member, Principles and Practices of Parallel Programming (PPoPP), 2013
- PC member, FMCAD 2013
- PC member, EuroMPI 2013

2012

- Member, NSF panel, 2012.

- Co-Guest Editor (with Shaz Qadeer), Special Issue of *Formal Methods in System Design* (Springer), Best Papers of Computer Aided Verification 2011, Vol. 41, No. 1, August 2012.
- PC member, EuroMPI 2012
- PC member, FM 2012
- PC member, Intl. Supercomputing Conference 2012 (Tutorials)
- PC member, Runtime Verification (RV) 2012
- External PhD thesis Committee Member, Dr. Fabio Mercurio, Univ. La Aquila, Italy, 2012.

2011

- External PhD thesis Committee Member, Dr. Cristian Rosa, LORIA, France, 2011.
- PC Member, ICS 2011, International Conference on Supercomputing, Phoenix, AZ
- PC Member, CCGrid 2011, IEEE/ACM International Symposium on Cluster, Cloud, and Grid Computing, Newport Beach, CA
- PC Member, MEMOCODE 2011, Methods and Models for Co-Design, Cambridge, UK, July 11-13, 2011
- PC Member, SOFTSEM 2011, Nový Smokovec, Slovakia, January 2011.
- PC Member, CAV 2011 (was also PC Co-Chair)

2010

- PC Member, FMCAD 2010, Formal Methods in Computer Aided Design, Austin, TX
- PC Member, PADTAD 2010, Workshop on Parallel and Distributed Systems: Testing, Analysis, and Debugging (PADTAD - VIII), July 12-13, Trento, Italy.
- PC Member, CAV 2010, Edinburgh, UK, July 15-19, 2010 (Formal Methods in Computer Aided Design).
- PC Member, EuroMPI 2010, The 17th EuroMPI Conference, Stuttgart, Germany, 12-15 September, 2010.
- PC Member, MEMOCODE 2010, Methods and Models for Co-Design, Grenoble, France, July 26-28, 2010.
- PC Member: PSTI 2010, Parallel Software Tools and Tool Infrastructures, September 13-16, San Diego (part of ICPP 2010).
- PC Member, PDMC 2010, 9th International Workshop on Parallel and Distributed Methods in Verification.
- PC Member, SPIN 2010, 17th Spin Workshop, Twente University, 27-29 September 2010.
- PC Member, FMCAD 2010, Formal Methods in Computer Aided Design, Lugano, Switzerland, October 20-23.

2009 AND BEFORE

- Tutorials Committee, Supercomputing Conference, Portland, OR, 2009.
- Program Committee, “Methods and Models for CoDesign, ” (MEMOCODE), 2009.
- Program Committee Member, Formal Methods in Computer-Aided Design (FMCAD), 2009.
- Program Committee Member, Formal Methods in Computer-Aided Design (FMCAD), 2000, 2002, 2004, 2006-2008.
- Program Committee, “Methods and Models for CoDesign, ” (MEMOCODE), 2005, 2006, 2007, 2008.
- Program Committee Member, Computer Aided Verification (CAV), 2000, 2006, 2007, 2008.
- Program Committee Member, Theorem-proving and Higher Order Logic (TPHOLs), Scotland, 2000, 2001, 2002, 2007-2008.
- Microsoft University Booth during Supercomputing, 2006, Tampa, Florida.
- Guest editor (with Warren Hunt as Co Guest-Editor), Special Issue of *Formal Methods in*

System Design (Kluwer), “Industrial Formal Methods in Hardware Design: A Sampling,” Vol. 22, No. 2, March 2003.

- Program Committee Member, International Conference on Advanced Research in Asynchronous Circuits and Systems. '99 to '02.
- Program Committee Member, CHARME (IFIP WG 10.2/10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods), 1999, 2001, 2003, 2005.
- Program Committee Member, International conference on computer design (ICCD), '00, '02.
- Member, Implementation/Verification Development Working Group (DWG) and On-Chip Bus DWG, Virtual Sockets Interface (VSI) Alliance. 1999.
- Member, IFIP WG 10.5, 1993-2000. Voluntarily resigned in 2000.
- Guest editor, Special Issue of *Formal Methods in System Design* (Kluwer), “Formal Methods for CAD: Enabling technologies and system-level applications,” Volume 16, Issue 1, January, 2000.
- Site Reviewer, 1999, NSF Science and Technology Center competition, SUNY, Stony Brook, NY.
- External MS thesis Committee Member, Michigan Technical University, 2005.
- External Ph.D. examiner, Dept of Computer Science (IRO), University of Montreal, Canada, 1999.
- Tutorials Chair, Async'99: Fifth International Conference on Advanced Research in Asynchronous Circuits and Systems, Barcelona, April 1999.
- Member, NSF panel, 2005.
- Member, NSF panel, 1998.
- Member of panel and session chair, Async'98: Fourth International Conference on Advanced Research in Asynchronous Circuits and Systems, San Diego, CA, March 1998.
- Session chair, session on “Formal Characterizations of Systems,” International Symposium on Computer Hardware Description Languages (CHDL), 1997, Toledo, Spain, April 1997.
- Program Committee Member, International Symposium on Computer Hardware Description Languages (CHDL), 1997, Spain.
- External Ph.D. examiner, Computer Science, University of Adelaide, 1997.
- External Ph.D. examiner, Dept of Computer Science (IRO), University of Montreal, Canada, 1996.
- Program Committee Member, International Symposium on Computer Hardware Description Languages (CHDL), 1995, Tokyo, Japan.
- Session co-chair, session on “Computer Representations for Verification,” International Symposium on Computer Hardware Description Languages (CHDL), 1995, Tokyo, Japan.
- External Ph.D. examiner, Electrical and Computer Engineering, University of Calgary, Canada, July 1995.
- External Ph.D. examiner, Computer Science, Monash University, Clayton, Australia, May 1995.
- Co-guest editor (with Erik Brunvand) of a special issue “Asynchronous Circuits: CAD Tools, and Significant Applications,” in *Integration, The VLSI Journal*, October 1993.
- Member of a panel discussion on “Why do Asynchronous Systems Matter?” during TAU '92: 1992 Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, Princeton, NJ, March 18–20, 1992.
- External Ph.D. examiner, Department of Computer Science, University of Glasgow, UK, Sep 13, 1991.

CONFERENCE TUTORIALS (Before 2016)

1. Matthias S. Müller, David Lecomber, Tobias Hilbrich, Mark O'Connor, Bronis R. de Supinski,

- and Ganesh Gopalakrishnan, “Efficient Parallel Debugging for MPI, Threads, and Beyond” **Full Day Tutorial, Supercomputing**, Salt Lake City, November 2016.
2. Matthias S. Müller, David Lecomber, Tobias Hilbrich, Mark O’Connor, Bronis R. de Supinski, and Ganesh Gopalakrishnan, “Efficient Parallel Debugging for MPI, Threads, and Beyond” **Full Day Tutorial, Supercomputing**, Austin, November 2015.
 3. Matthias S. Müller, David Lecomber, Tobias Hilbrich, Mark O’Connor, Bronis R. de Supinski, and Ganesh Gopalakrishnan, “Efficient Parallel Debugging for MPI, Threads, and Beyond” **Full Day Tutorial, Supercomputing**, New Orleans, November 2014.
 4. Tobias Hilbrich, Ganesh Gopalakrishnan, Matthias S. Müller, Bronis R. de Supinski, David LeComber, “Debugging MPI and Hybrid/Heterogeneous Applications at Scale,” **Full Day Tutorial, Supercomputing**, Denver, November 2013.
 5. Tobias Hilbrich, Ganesh Gopalakrishnan, Matthias S. Müller, Bronis R. de Supinski, David LeComber, “Debugging MPI and CUDA at Scale,” **Full Day Tutorial, Supercomputing**, Salt Lake City, Nov, 2012.
 6. (Half Day Tutorial), Ganesh Gopalakrishnan, “Symbolic Analysis of GPU Programs for Correctness and Performance,” Formal Methods 2012, Paris.
 7. (Tutorial), Ganesh Gopalakrishnan, “Safe March to Extreme-Scale Computing aided by Formal Methods,” SJTU HPC Center, Shanghai Jiaotong University, May 2012.
 8. Invited tutorial (2 one-hour lectures), UPMARC Summer School, Böson, Sweden, June 2011.
 9. Tobias Hilbrich, Ganesh Gopalakrishnan, Matthias S. Müller, Bronis R. de Supinski, David LeComber, “Scalable Dynamic Formal Verification and Correctness Checking of MPI Applications,” **Full Day Tutorial, Supercomputing**, Seattle, Nov, 2011.
 10. Ganesh Gopalakrishnan, Matthias S. Müller, and Bronis R. de Supinski, “Scalable Dynamic Formal Verification and Correctness Checking of MPI Applications,” **Half Day Tutorial, Supercomputing**, New Orleans, Nov 15, 2010.
 11. Ganesh Gopalakrishnan, “Tutorial: Dynamic Verification of Message Passing and Threading,” PPOPP, Bangalore, January 2010.
 12. Ganesh Gopalakrishnan, Sarvani Vakkalanka, and Yu Yang, “Practical Formal Verification of MPI and Thread Programs,” Full Day Tutorial at PPOPP, Raleigh, February 2009.
 13. Ganesh Gopalakrishnan, “Tutorial T8: Practical Formal Verification of MPI and Thread Programs,” ICS, Yorktown Heights, June 2009.
 14. Ganesh Gopalakrishnan, “Tutorial 03: Practical MPI and Pthread Dynamic Verification,” FM 2009, Eindhoven, November 2009.
 15. Invited full-day tutorial: Practical Formal Verification of MPI and Thread Programs, Nov 2009. EuroPVM/MPI, Espoo.
 16. Ganesh Gopalakrishnan and Yu Yang, “Runtime Model Checking of Multithreaded C Programs using Automated Instrumentation Dynamic Partial Order Reduction and Distributed Checking,” Half Day tutorial at *FM’08: 15th International Symposium on Formal Methods*, May 26 - 30, 2008, Abo Akademi University, Turku, Finland.
 17. Invited Tutorial, “Specification and Verification of Shared Memory Protocols and Consistency Models,” Ching Tsun Chou - Intel Corporation, Steven German - IBM T.J. Watson Research Center, and Ganesh Gopalakrishnan - University of Utah, FMCAD 2004.
 18. “Foundations of Theorem Proving,” a two-day course offered at Intel Corporation, Jones Farm Campus, Oregon, May 24-25, 2000.

ADDITIONAL INVITED TALKS/PANELS

1. 2022: 10-minute Random Access Talk, Ganesh Gopalakrishnan, “The sorry state of Data Race Checking in Parallel Programming, and Some Promising Directions,” Programming Systems Research Symposium (virtual), Feb 28-Mar 3, 2022.

2. 2018: Keynote lecture, “Making Formal Methods for HPC Disappear,” Correctness 2018: Second International Workshop on Software Correctness for HPC Applications, Held in conjunction with SC’18.
3. 2018: Distinguished Lecture, Department of Computer Science, University of California, Davis (May 10, “Can Formal Methods (alone) Rescue HPC Debugging?”)
4. May 2, 2018: “Can Formal Methods (alone) Rescue HPC Debugging?,” Colloquium at the Department of Computer Science, University of Delaware.
5. Panelist, workshop on “Computational Reproducibility at Exascale 2017 (CRE2017),” Supercomputing 2017, Denver, CO.
6. Invited speaker, “Formal Methods for HPC: Correct Dosage,” Software Engineering for Computational Science and Engineering on Supercomputers (SC16 BOF)
7. Panel on reproducibility at SC’16: Different architectures, different times: Reproducibility and repeatability in high performance computing, 2016. Moderators: Miriam Leeser and Michela Taufer.
8. “Bugs: Black Ice on Parallel Roads,” delivered at three locations:
 - (a) University of British Columbia.
 - (b) Aalto University, Helsinki, Finland.
9. Invited Speaker, Challenges in 21st Century Experimental Mathematical Computation (July 21-25, 2014), Providence, RI.
10. Invited talk, Microsoft Research, Redmond, WA, May 2014.
11. Invited talk, Pacific Northern National Laboratory, Richland, WA, May 2014.
12. Invited colloquium at Washington University, St. Louis, November 2013.
13. Invited colloquium at IISc Bangalore, India, June 2013.
14. Invited talk at Microsoft Research, Bangalore, India, June 2013.
15. Invited talk, “Formal Correctness Methods at the Million CPU Scale,” Infinity (FM 2012 Conference Workshop), Paris, August 2012.
16. Invited talk, “Symbolic Formal Analysis of GPU Programs,” Intel Bangalore, June 2012.
17. Invited talk, Haifa Verification Seminar, sponsored by Intel, Sep 2011.
18. Invited member of panel in the Indo/US Workshop on High Performance Computing held prior to the Principles and Practices of Parallel Programming (PPoPP) and High Performance Computer Architecture (HPCA) conferences held in Bangalore, January 9-10, 2010.
19. Ganesh Gopalakrishnan, “Dynamic Verification Methods for Message Passing Systems,” Microprocessor Testing and Verification Workshop, Austin, December 2009.
20. Ganesh Gopalakrishnan, “Practical Formal Verification of MPI and Thread Programs,” given at Intel Corporation, Santa Clara, CA, May 4, 2009.
21. Ganesh Gopalakrishnan, “Practical Formal Verification of MPI and Thread Programs,” given at the Helsinki University of Technology, November 2009 (Host: Prof. Keijo Helijanko).
22. Ganesh Gopalakrishnan, “Dynamic Verification Methods for Message Passing Systems” given at the Dagstuhl Summer School on Concurrency and Formal Methods in 2009 organized by Shaz Qadeer (MSR), Cormac Flanagan (UCSC), and Madhusudan Parthasarathy (UIUC).
23. “Inspect, ISP, and FIB: reduction-based verification and analysis tools for concurrent programs,” talk given at Microsoft Research, Bangalore, India, June 6, 2008.
24. “In-Situ Model Checking of MPI Parallel Programs,” talk presented at Microsoft Research, Redmond, WA, August 27, 2007.
25. “Formal Analysis for Debugging and Performance Optimization of MPI,” talk presented at Microsoft, Redmond, WA, March 2, 2007.
26. “Formal Verification of High Performance Computing Software,” talk given at Microsoft Research, Bangalore, India, June 29, 2006.
27. “Formal Methods for Hierarchical Protocols in Shared Memory Multiprocessors,” talk given

- at Intel Corporation, Bangalore, India, June 30, 2006.
28. “Verifying MP Executions against Itanium Orderings using SAT,” Formal Verification Research Symposium, Intel Corporation, June 11, 2004; then again as a Colloquium at the University of Calgary in July 2004.
 29. “Formal Verification Research at Utah,” Weizmann Institute of Technology, Rehovot, Israel, June 2001.
 30. “Verification of Weak Shared Memory Coherence Protocols,” Strategic CAD Laboratories, Intel Corporation, May 26, 2000.
 31. Invited presentation at the Intel Validation Summit, “Verification of I/O Protocols Through Model-Checking and Refinement,” Santa Clara, May 9, 2000.
 32. Invited presentation at the Intel Validation Summit, “Verification of Coherence Protocols against Shared Memory Consistency Models using Test Model-checking,” Santa Clara, November 12, 1999.
 33. “Verification of Weak Shared Memory Coherence Protocols,” Strategic CAD Laboratories, Intel Corporation, May 26, 2000.
 34. Research Seminar “Verification of Coherence Protocols for Conformance to Memory Consistency Models using ‘Test Model-Checking’,” research seminars given at
 - (a) University of Texas, Austin, TX, December 9, 1999.
 - (b) Intel, Austin, TX, December 10, 1999.
 - (c) Intel, Santa Clara, CA, November 12, 1999.
 35. Research Seminar “Formal verification of shared memory systems during their Design,” at the University of Pisa, July 6, 1999.
 36. Research seminar on Formal Verification, Silicon Automation Systems, Bangalore, India, June 29, 1999.
 37. Research Seminar “Formal verification of shared memory systems during their design,” University of Montreal, June 22, 1999.
 38. Invited talk “Formal verification of shared memory systems during their design” at the workshop Hardware Design and Petri Nets (part of Petri Nets’99), Williamsburgh, VA, June 20, 1999.
 39. Invited talk “A Complete Method for Verifying Sequential Consistency of Shared Memory Systems,” Stanford Research Institute (SRI) International, Menlo Park, CA, June 16, 1999.
 40. “Formal verification of Conformance to Memory Models,” talk in a research workshop given at LORIA, Nancy, France, April 23, 1999.
 41. “Formal verification of Conformance to Memory Models,” invited talk given at the Dept. of Computer Science, University of Austin, October 1999.
 42. “1-day Tutorial on Formal Methods,” given at the Indian Institute of Technology, Bombay, India, and the Indian Institute of Science, Bangalore, India, June/July, 1998.
 43. “The Utah Verifier Project,” presented at Stanford University, Nov 17, 1997.
 44. “Formal Methods work in the Utah Verifier group,” talk at the Naval Research Labs, Washington D.C., Nov 3, 1997.
 45. “Applying Formal Methods to System Level Hardware Designs,” colloquium at the University of Montreal, April 8, 1997.
 46. “Applying Formal Methods to System Level Hardware Designs,” presented at Sun Microsystems Laboratories, Menlo Park, March 4, 1997.
 47. “The Avalanche Scalable Parallel Processor: An Overview of its Design and Formal Validation,” given at
 - (a) Hewlett-Packard Laboratories, Palo Alto, CA, July 9, 1996.
 - (b) Hewlett-Packard General Systems Laboratories, Roseville, CA, Feb 12, 1996.
 - (c) University of California, Davis, Feb 13, 1996.

- (d) Stanford Research Institute, Feb 15, 1996.
- 48. "Some Experiments with Explicit Enumeration," Invited talk at the Workshop on Higher-Order Logic Theorem Proving and Its Applications, Aspen Grove, UT, USA. September, 1995.
- 49. "Specification Driven Design of Hardware," Computer Science Department, University of Calgary, November 29, 1991.
- 50. "Design and Verification of the Roll Back Chip," Computer Science Department, University of Glasgow, Glasgow, Scotland, U.K., September 12, 1991.
- 51. "Combining Verification and Simulation," Computer Science Department, University of Waterloo, Waterloo, Canada, July 5, 1991.
- 52. "Combining Verification and Simulation," Computer Science Department, Indian Institute of Science, Bangalore, India, December, 1990.
- 53. "Combining Verification and Simulation," Computer Science Department, University of Oregon, Eugene, OR, November, 1990.
- 54. "A Process Model for Synchronous Hardware," at the Computer Science Departments of:
 - (a) University of Indiana, Bloomington, April 5, 1990;
 - (b) University of Montreal, Montreal, Canada, April 3, 1990;
 - (c) SUNY Albany, April 2, 1990.
- 55. "Formalization of an Operational Approach to Hardware Specification and Validation," Invited talk given at the 1989 Banff Workshop on Type Theory and Higher Order Logic, Graham Birtwistle (organizer), Banff Centre, Canada, September 13–28.
- 56. "Hardware Specification and Validation Using HOP," Laboratory for Automation, Communication, and Information Systems Research, Department of Computer Science, University of Victoria, Vancouver, British Columbia, Canada, July 28, 1989.
- 57. "Specification of Pipelined Hardware in HOP," Computer Science Department, Simon Fraser University, Burnaby, British Columbia, April 1989.
- 58. "HOP: A Language for Specification, Verification and Design Automation," given at the Micro-electronics and Computer Corporation (MCC), Austin, Texas, January 1988.
- 59. Ten job-interview related talks.

OUTREACH AND VOLUNTARY SERVICE

1. Judge for the Salt Lake Valley Science and Engineering Fair (SLVSEF), 2010, 2009.
2. Gave three 30-min talks in the College of Engineering Day entitled "Have you hugged your computer lately?" on October 26, 2008.
3. Hosted a colloquium, "Outreach, Diversity, and Recruiting Issues in Computing," School of Computing, January 10, 2007.
<http://www.cs.utah.edu/dept/colloq/05-06colloq/outreach.html>.
4. Co-Hosted (with Rajeev Balasubramoniam) the "Multicore Discussion Colloquium," November 5, 2007.
<http://www.cs.utah.edu/arch-rd-web/index.php?n=Main.Colloq>.
5. Host, Club U, College Days (Half-day science lectures and experimental demonstrations to visiting middle-school students), University of Utah, July 2006 and July 2007.
6. Two one-hour science presentations to the ELEAP Class, University of Utah, November 2007.
7. Presentations in the Academy of Info Technology Region Activity, March 2007 and March 2008, Larry H. Miller SLCC Campus, South Jordan (Visit and half-day technical presentations with Computer Engineering senior students addressing high-school students).
8. Host, West High Girls' Math Club student visit, 2006-2007 (hosting visit of student groups)
9. Science Project Mentoring for two students from West High-School, October 2007.
10. MACROS: Summer Science Camp for middle-school children.

BEST PAPER AWARDS

1. Subodh Sharma and Ganesh Gopalakrishnan, “Formal Verification of MCAPI Applications Using Dynamic Verification Tool MCC,” Best Paper in Verification Session, TECHCON, 2009, Austin.
2. Robert Palmer, Ganesh Gopalakrishnan and Robert M. Kirby, “Semantics Driven Dynamic Partial-Order Reduction of MPI-based Parallel Programs,” Proceedings of Parallel and Distributed Systems: Testing and Debugging (PADTAD), London, England, July 9, 2007. Won the Best Paper award.
3. Robert Palmer, Michael DeLisi, Ganesh Gopalakrishnan and Robert M. Kirby, “An Approach to Formalization and Analysis of Message Passing Libraries,” Proceedings of the 12th International Workshop on Formal Methods for Industrial Critical Systems (FMICS), Berlin, Germany, July 1-2, 2007. Won the EASST (European Association of Software Science and Technology) Best Paper Award.
4. Xiaofang Chen, Steven M. German and Ganesh Gopalakrishnan, “Transaction Based Modeling and Verification of Hardware Protocols,” TECHCON, Lake Buena Vista, FL, 2007. Best Paper in Verification Session.
5. Salman Pervez, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, and William Gropp, “Formal Verification of Programs that use MPI One-sided Communication,” Outstanding Paper, Recent Advances in Parallel Virtual Machine and Message Passing Interface (EuroPVM/MPI), Bonn, Germany, 2006, LNCS 4192, 30-39.

RESEARCH GRANTS (Before 2017)

1. PI: CCF: SHF: Medium: Collaborative: *A Static and Dynamic Verification Framework for Parallel Programming*. (CCF 1302449, 4-15-13 to 4-14-17, \$400,000). Collaborators: Vivek Sarkar and Eric Mercer (1-year no-cost extension)
2. (PI) CCF 1218835 CPA-DA: Formal Methods for Multi-core Shared Memory Protocol Design, 06/13/2012 12/19/2011 \$16,000.00, Sankar Basu
3. (PI), University Teaching Committee, \$3,500 to develop concurrency curricula
4. (PI), NSF/IEEE TCPP, \$1,000 plus \$5,000 of Nvidia GPU hardware
5. (PI), University Research Committee, \$2,500 for building a GPU cluster using hardware obtained from the NSF/IEEE TCPP award
6. Faculty Associate, SUPER (Institute on Sustainability and Resilience), DOE
7. (PI) CCF 1118485 Travel and Registration Support for Computer Aided Verification 2011, 04/07/2011 12/29/2010 \$7,000.00, Nina Amla
8. PI, CCF FRS (Failure Resistant Systems) : Localized, Layered Formal Hardware/Software Resilience Methods (CCF 1255776)
9. PI (Co-PI is Zvonimir Rakamaric), \$219,999 (NSF) and \$77,000 (SRC).
10. PI, SI2-SSE: Correctness Verification Tools for Extreme Scale Hybrid Computing (ACI-1148127), NSF, \$444,278.
11. Co-PI (Zvonimir Rakamarić is PI), EAGER: Memory Models: Specification and Verification in a Concurrency Intermediate Verification Language (CIVL) Framework (CCF 1346756), NSF, \$300,000.
12. (Co-PI) CNS 1035658 CPS: Medium: Safety-Oriented Hybrid Verification for Medical Robotics, 09/02/2010 03/11/2010 \$500,000.00, Mohamed G. Gouda
13. A Sun 8-core server was donated to our group by Sun Microsystems. This high-end server is being used in a parallel computing class currently being taught by Berzins. Continued use of this very capable computing resources is anticipated.
14. Two NSF REU supplements totaling \$32,000 (received in 2009).

15. NSF CCF-0903408, "Collaborative Research: MCDA: Formal Analysis of Multicore Communication APIs and Applications," \$188,299 (total amount) awarded in 2009 under a new NSF program called MCDA (SRC/NSF collaboration).
16. SRC TJ 1993, "Formal Analysis of Multicore Communication APIs and Applications," received \$15,000 for year-1 in 2009 (years 2,3 remaining; part of the above MCDA where NSF paid the above amount and SRC pays this amount).
17. LLNL/DOE, "Static Analysis using Rose," \$13,410, 2009.
18. \$1,000 to run PADTAD 2009, received from Microsoft Research.
19. Gift, Microsoft Research, 2009.
20. Gift, Microsoft Research, 2008.
21. PI, "Formal Methods for Multi-core Shared Memory Protocol Design," NSF Grant CCF 0811429, \$268,843. Awarded in 2008. Active June 2008 - May 2011.
22. PI (with Co-PI Rajeev Balasubramoniam), "Formal Specification, Verification, and Test Generation for Multi-core CPUs," SRC Contract 2008 TJ 1847, \$187,291. Awarded in 2008. Active November 2008 - October 2011.
23. NSF REU supplement \$6,000 (received April 2008).
24. Plaque awarded by Microsoft to Gopalakrishnan and Kirby at Supercomputing 2007 in recognition of our group's "Early contributions to Microsoft's Windows Compute Cluster Server 2003, and Charter Membership of the Microsoft High Performance Computing Institute Program."
25. Co-PI (with Rajeev Balasubramoniam being PI), University of Utah Seed Grant, \$30,000.
26. NSF REU supplement \$6,000 (received April 26, 2006).
27. \$2,000 to run TV'06 workshop (gift from Microsoft), August 2006.
28. Ganesh Gopalakrishnan and Robert M. Kirby, "Formal Analysis and Code Generation Support for MPI," Microsoft HPC Institute \$519,000 (three years), starting February 2006. Cluster supplement of \$30,000 added in 2006.
29. Ganesh Gopalakrishnan (PI) and Robert M. Kirby (Co-PI), "CSR-SMA: Toward Reliable and Efficient Message Passing Software Through Formal Analysis," \$400,000 for four years, starting August 2005.
30. Ganesh Gopalakrishnan (PI), "Scaling Formal Methods Towards Hierarchical Protocols in Shared Memory Processors," Semiconductor Research Corporation (SRC) Contract 2005-TJ-1318, \$300,000.
31. University of Utah Teaching Committee, 2005, \$4,000 towards developing course on formal methods and security.
32. Semiconductor Research Corporation - Principal Investigator (with Co-PI Konrad Slind), "Verification of Shared Memory Consistency Protocols," \$240,000, for 09/01/2002 - 08/31/2004.
33. NSF - Principal Investigator (with Co-PI Konrad Slind and International Collaborator Michael J.C. Gordon), "ITR: Protocol Synthesis and Verification," \$259,982, for 10/01/2002 - 9/30/2005.
34. NSF - Co-Principal Investigator (Erik Brunvand recently made PI), "Microengines for Programmable Self-timed Control," \$412,914 for 7/1/2000 - 6/30/2003.
35. NSF - Principal Investigator (with Gary Lindstrom as equal Co-PI and Dominique Méry as international collaborator), "ITR/SW: Formal Methods for Robust Embedded Software," \$428,737, for 10/01/2000 - 9/30/2003.
36. NSF - Principal Investigator "Formalization and Verification of Computer System Interconnect Busses," \$348,114, for 07/01/2000 - 06/30/2003.
37. Intel Corporation - Principal Investigator, "Test Model-checking Based Verification of Multi-processor Cache Coherence Protocols," \$50,000 for 07/01/2000 - 06/30/2001.
38. Intel Corporation - Principal Investigator, "Test Model-checking Based Verification of Multi-

- processor Cache Coherence Protocols,” Equipment Grant for \$22,000, 07/01/2000.
39. University of Utah - '99 - \$37,500 for upgrading the FPGA array board of our IKOS Hermes hardware emulator.
 40. NSF - '99: \$9,000, Principal Investigator. Equipment supplement for CCR-9800928 (below).
 41. NSF - '99: \$30,241, Principal Investigator. One graduate student supplement for CCR-9800928 (below) has recently been approved.
 42. NSF - '98: \$10,000, Co-Principal-Investigator (with Erik Brunvand). Research Experience for Undergraduates (REU) supplement.
 43. Digital Equipment Corporation (Compaq) - '98: \$12,000, Principal Investigator. Cash award, 1998.
 44. NSF - '98: \$255,000, Principal Investigator. “Formal Verification and Design of System-Level Hardware,” Grant No. CCR-9800928, \$82,953 for FY98. Remaining during FY99.
 45. NSF - '97: \$9,758, Principal Investigator. “Formal Methods for Secure and Reliable Hardware/Software Design,” Western Europe Program (NSF), 1997. Travel Award.
 46. NSF - '96: \$492,738. Co-Principal-Investigator (with Erik Brunvand). “Application-Driven Advancement of Asynchronous Design Methods.” 1996-99.
 47. DARPA - '96: \$320,000, Principal Investigator. “Towards Applying Hardware Verification Techniques to Industrial-Scale Problems,” DARPA order number BAA 96-07, #580. Project codename: Utah Verifier (“UV”). 1997-99.
 48. NSF - '95: \$5,000, Principal-Investigator. Research Experience for Undergraduates (REU) supplement.
 49. DARPA - '94: \$78,000, Faculty Associate. “Communication and Memory Architectures for Scalable Parallel Computing.” ARPA award. PIs: Alan Davis and John Carter. Support: Two summer months (self) and RA-ship (Ratan, PhD student) for the award period (3 years).
 50. NSF - '94: \$104,861, Principal Investigator. “A multi-paradigm verification system tailored for the design refinement cycle,” NSF MIP-9321836. September 1994 to August 1997.
 51. NSF - '94: \$15,000, Principal Investigator. Equipment supplement to MIP-9321836.
 52. NSF - '94: \$12,230, Co-Principal Investigator (with Erik Brunvand and Steve Nowick). “Symposium on Advanced Research in Asynchronous Circuits and Systems.”
 53. University of Utah Teaching Committee - '94: \$4,000 towards release time. “Formal Methods in Undergraduate Computer Engineering Education.”
 54. NSF - '92: \$240,374, Co-Principal Investigator (with Erik Brunvand). “The Design of Asynchronous Circuits and Systems with Emphasis on Correctness and Proven Optimizations,” NSF MIP-9215878.
 55. NSF - '92: \$5,000, Co-Principal-Investigator (with Erik Brunvand). Research Experience for Undergraduates (REU) supplement.
 56. University of Utah Research Council - '92: \$5,000, Principal Investigator. “Reordering Queues: Special Purpose Hardware for Optimizing Instruction Sequences.”
 57. University of Utah - '91: \$5,000 equipment match.
 58. NSF - '90: \$2,000 supplement for VLSI fabrication.
 59. NSF - '89: \$260,726, Principal Investigator. “Towards Making the Specification Driven Design of Custom Hardware Practical.” MIP-8902558.
 60. University of Utah Research Council - '89: \$5,000, Principal Investigator. “A Unified Approach to the Specification Driven Design of Custom Hardware.”
 61. NSF - '87: \$60,000, Principal Investigator. “Behavior and Protocol Specification of VLSI Systems for Verification and Automation.” Research Initiation Award MIP-8710874. 9/87 to 8/90.
 62. SIGDA - '89-91: \$3,000, Principal Investigator. Honorable mention, and library awards.

SUPERVISION OF POST DOCTORAL FELLOWS/STAFF

1. Ian Briggs, Research Staff Member, 2016 till present.
2. Dr. Alexey Solovyev, 2013 till 2016.
3. Dr. Diego Oliveira, 7/2012 - 5/2014.
4. Dr. Igor Melatti, from 7/2005 till 12/2005. Also summer of 2006.
5. Dr. Abdel Mokkedem, from 7/1997 till 6/1999 (est). Working for Intel corp.

THESIS MS COMMITTEES CHAIRED

1. 2014, Tyler Sorensen.
2. 2010, Wei-Fan Chiang.
3. 2010, Ben Meakin.
4. 2008, Salman Pervez,
5. 2004, Hemanth Sivarajkumar.
6. 2002, Prosenjit Chatterjee.
7. 1999, Rajnish Ghughal.
8. 1992, Prabhakar Kudva.
9. 1992, Prabhat Jain.
10. 1989, Narayana Mani.

BS and NON-THESIS MS

- 2020, Harvey Dam (BS at Utah; MS at GaTech)
- 2014, Leif Andersen.
- 2014, Bruce Bolick.
- 2010, Joe Mayo.
- 2010, Brandon Gibson.
- 2010, Grant Ayers.
- 2009, Alan Humphrey
- 2009, Carson Jones.
- 2009, Chris Derrick.
- 2006, Sonjong Hwang.
- Richard Sharp, Robert Palmer, Ben Prather, Omid Saadati, Jacob Tripp, Steve Barrus, Eun Yong Kang, Michael DeLisi.

NEW COURSES

- CS 5955, “Practical Parallel and Concurrent Programming,” Co-taught with the RiSE team, Microsoft Research, Fall 2010.
- CS 5966, “Multi-core Computing” taught during Spring 2009 on the fundamentals of concurrency.
- CPSC 7930, “Turing Seminar,” – ran a successful seminar for new students, involving reading Turing Award papers, Fall 2005.
- CPSC 6940, A Graduate Sampler class. Fall 2003.
- CPSC 6933, Hardware Emulation: W99-semester
- CS 611, Formal Methods for System Design: F96, 97
- CS 573, Logic for Computer Science: S93.
- CS 611, Program Verification: F86, F87, F89, F90, F91, F93, F94 and W92
- CS 570, High Level Synthesis of VLSI: F91.
- CS 577, Asynchronous Systems: W90.

COURSE TEACHING VARIETY

1. CS 2000, Programming in C, F 08.
2. CS 2100, Discrete Structures, S’13, F’13
3. ECE/CPSC 3700, Fundamentals of Digital Design, 2004, 2006.

4. ECE/CPSC 3710, Microprocessor Design Laboratory, 2004, 2006.
5. CPSC 6100, Foundations of Computer Science: F98, F99, F00, F01, S05
6. CPSC 6110, Formal Methods in System Design: F99, F00, F01, F02, F04, S'14
7. CPSC 3100, Models of Computation, S00, S01, S02, F'12, F'13
8. CS 511, Programming Languages: S98
9. CS 505, Introduction to Theoretical Computer Science: W98
10. EE/CS 552, Microprocessor Design Laboratory: S97
11. EE/CS 551, Microprocessor Laboratory: W97
12. CS 511, Programming Linguistics: S90, S91, S95
13. EE/CS 564, Microprocessor Design Laboratory: S95
14. CS 561, Advanced Computer Organization: W93
15. CS 506, Operating Systems: W87, F92.
16. CS 507, Compilers: S92
17. CS 541, Modeling Integrated Circuits: W91
18. CPSC 463 (Calgary) VLSI Design: W89
19. CPSC 433 (Calgary) Inference and Automation of Reasoning (Prolog): F88
20. CS 451, Software Engineering Laboratory series: F87, W88, S88

UNIV. and COLLEGE COMMITTEES

- University Diversity Committee, 2011-2013.
- College Retention, Promotion, and Tenure Committee Representative from the School of Computing, 2001-02, 2004, 2008, 2010-2011 (as Chair), 2011-2012 (as member).
- 1990-92: College Council representative for CS.

DEPARTMENT COMMITTEES

2020-2021

1. Director of Graduate Studies.
2. University of Utah Academic Senate.

2018-2020

3. Director of Graduate Studies.

2015

4. Organizer, Organick Memorial Lecture Committee, 2012 till 2019.

Prior to 2015

5. Chairman, Retention, Promotion, and Tenure Committee, 2014.
6. Chairman, Retention, Promotion, and Tenure Committee, 2013.
7. Organizer, Organick Memorial Lecture Series, 2012, 2013.
8. 2009-12: Colloquium Committee Chair
9. 2006-09: Outreach, Colloquium
10. 2007-09: Graduate Admissions
11. 2010-11: Colloquium
12. 2005-06: Colloquium, Undergraduate Studies
13. 2004-05: Undergraduate Studies
14. 2003-04: Graduate Admissions
15. 2001-02: Member, Graduate Studies Committee
16. 2000-01: Member, Graduate Studies Committee
17. 1999-00: Assoc Chair for Research, Department of Computer Science.
18. 1999-00: Member of the Graduate Admissions and Comprehensive Exams Committees.
19. 1998-99: Director of Graduate Admissions, Comprehensive Exams.
20. 1997-98: Departmental RPT Chair, Comprehensive Exams.

21. 1996-97: Computer Engineering, Computer Policies.
22. 1994-95: Undergraduate, Computer Engineering.
23. 1993-94: Undergraduate, Computer Engineering.
24. 1992-93: Colloquium chair.
25. 1990-92: Graduate Committee.
26. 1989-90: Faculty Recruiting, Curriculum.
27. 1987-88: Grad. Admissions.
28. 1986-94: Library representative for the Department.

REFEREED JOURNAL ARTICLES: PRIOR TO 2017

1. Alan Humphrey, Qingyu Meng, Martin Berzins, Diego Caminha B De Oliveira, Zvonimir Rakamaric, Ganesh C. Gopalakrishnan, "Systematic Debugging Methods for Large Scale HPC Computational Frameworks," *Computing in Science & Engineering*, no. 1, pp. 1, 2014. PrePrints PrePrints, doi:10.1109/MCSE.2014.11
2. Ganesh Gopalakrishnan, Robert M. Kirby, Stephen Siegel, Rajeev Thakur, William Gropp, Ewing Lusk, Bronis R. de Supinski, Martin Schulz, and Greg Bronevetsky, "Formal Analysis of MPI-Based Parallel Programs: Present and Future," *Communications of ACM*, December 2011.
3. Guodong Li, Robert Palmer, Michael DeLisi, Ganesh Gopalakrishnan, and Robert M. Kirby, "Formal Specification of MPI 2.0: Case Study in Specifying a Practical Concurrent Programming API," *Science of Computer Programming*, 76(2), Elsevier, 2011, pp. 65-81, *Note: Electronic Edition Available in 2010 itself, at DOI URL <http://dx.doi.org/10.1016/j.scico.2010.03.007>*.
4. Yu Yang, Xiaofang Chen, Ganesh Gopalakrishnan and Robert M. Kirby, "Distributed dynamic partial order reduction," *Journal on Software Tools for Technology Transfer*, Volume 12, Issue 2 (2010), Page 113-122.
5. Salman Pervez, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, and William Gropp, "Formal methods applied to high performance computing software design: a case study of MPI one-sided communication based locking," *Software: Practice and Experience*, Published online December 2009, Hardcopy issue is 2010: Vol 40, Issue 1, Pages 23-43.
6. Xiaofang Chen, Yu Yang, Ganesh Gopalakrishnan, and Ching-Tsun Chou, "Efficient Methods for Formally Verifying Safety Properties of Hierarchical Cache Coherence Protocols," *Formal Methods in System Design*, Volume 36, Number 1, February, 2010, Pages 37-64.
7. Igor Melatti, Robert Palmer, Geoffrey Sawaya, Yu Yang, Robert M. Kirby, and Ganesh Gopalakrishnan, "Parallel and distributed model checking in Eddy," *STTT* 11(1): 13-25 (2009).
8. I. Melatti, R. Palmer, G. Sawaya, Y. Yang, R. M. Kirby, and G. Gopalakrishnan, "Parallel and distributed model checking in Eddy," *Journal International Journal on Software Tools for Technology Transfer (STTT)*, Springer Berlin / Heidelberg, ISSN 1433-2779 (Print), November 2008. (Special section on SPIN.)
9. Robert Palmer, Steve Barrus, Yu Yang, Ganesh Gopalakrishnan, and Robert M. Kirby, "Gauss: A Framework for Verifying Scientific Computing Software," *Electr. Notes Theor. Comput. Sci.* 144(3): 95-106 (2006).
10. Ali Sezgin and Ganesh Gopalakrishnan, "On the definition of sequential consistency," *Inf. Process. Lett.* 96(6): 193-196 (2005).
11. Annette Bunker, Ganesh Gopalakrishnan, and Konrad Slind, "Live sequence charts applied to hardware requirements specification and verification," *STTT* 7(4): 341-350 (2005).
12. Yue Yang, Ganesh Gopalakrishnan, and Gary Lindstrom, "UMM: an operational memory model specification framework with integrated model checking capability," *Concurrency and Computation: Practice and Experience*. Volume 17, Issue 5-6, Pages 465-487, February 2005.

13. Annette Bunker, Ganesh Gopalakrishnan, and Sally A. McKee, "Formal Hardware Specification Languages for Protocol Compliance Verification." *ACM Transactions on Design Automation of Electronic Systems*, vol. 9, no. 1, January 2004.
14. Hemanthkumar Sivaraaj and Ganesh Gopalakrishnan, "Random Walk Based Heuristic Algorithms for Distributed Memory Model Checking," *Electr. Notes Theor. Comput. Sci.* 89(1): (2003).
15. Ravi Hosabettu, Ganesh Gopalakrishnan, and Mandayam Srivas, "Formal Verification of a Complex Pipelined Processor," *Formal Methods in System Design*, Volume 23, Number 2, September 2003, pp. 171-213.
16. Ravi Hosabettu, Ganesh Gopalakrishnan, and Mandayam Srivas, "A Practical Methodology for Verifying Pipelined Microarchitectures," *IEEE Design & Test*, Volume 20, Number 4, July-August 2003, pp. 4-15.
17. Ratan Nalumasu and Ganesh Gopalakrishnan, "An Efficient Partial Order Reduction Algorithm with an Alternative Proviso Implementation," *Formal Methods in System Design* (Kluwer), Vol. 20, No. 3, May 2002, pp. 231-247.
18. Ratan Nalumasu and Ganesh Gopalakrishnan, "Deriving Efficient Cache Coherence Protocols Through Refinement," *Formal Methods in System Design* (Kluwer), Vol. 20, No. 1, January 2002, Pages 107-125.
19. Abdel Mokkedem, Ravi M. Hosabettu, Michael D. Jones and Ganesh C. Gopalakrishnan, "Formalization and Proof of a Solution to the PCI 2.1 Bus Transaction Ordering Problem," in special issue 'Formal Methods for CAD: Enabling technologies and system-level applications,' *Formal Methods in System Design*, Ganesh Gopalakrishnan (Editor.), Volume 16, Issue 1, January, 2000, pp. 93-119.
20. Hans M. Jacobson and Ganesh Gopalakrishnan, "Application-Specific Programmable Control for High-Performance Asynchronous Circuits," *Invited Paper, Proceedings of IEEE*, Vol. 87, No. 2, Feb 1999, pp. 319-331.
21. Jae-tack Yoo, Ganesh Gopalakrishnan, and Kent Smith, "Timing Constraints for High Speed Counterflow-Clocked Pipelining," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 7, No. 2, June 1999, pp. 167-173.
22. Prabhakar Kudva, Ganesh Gopalakrishnan, and Erik Brunvand, "Peephole Optimization of Asynchronous Macromodule Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 7, No. 1, March 1999, pp. 30-37.
23. Jae-tack Yoo, Kent Smith, and Ganesh Gopalakrishnan, "A Fast Parallel Squarer Based on Divide-and-Conquer," *IEEE Journal of Solid-state Circuits*, Vol. 32, No. 6, June 1997, pp. 909-912.
24. Venkatesh Akella and Ganesh Gopalakrishnan, "CFSIM: A Concurrent Compiled Code Functional Simulator for hopCP," *International Journal of Computer Simulation*, Vol. 4, No. 4, 1994, pp. 375-394.
25. Ganesh Gopalakrishnan, "Micropipeline Wavefront Arbiters using Lockable C-elements," *IEEE Design & Test of Computers*, Winter 1994, Vol.11, No.4, pp. 55-64.
26. Venkatesh Akella and Ganesh Gopalakrishnan, "Specification and Validation Control Intensive ICs in hopCP," *IEEE Transactions on Software Engineering*, Vol.20, No.6, June 1994, pp. 405-423.
27. Prabhat Jain and Ganesh Gopalakrishnan, "Efficient Symbolic Simulation Based Verification Using the Parametric Form of Boolean Expressions," *IEEE Transactions on Computer Aided Design*, Vol.13, No.8, August 1994, pp. 1005-1015.
28. Ganesh Gopalakrishnan, Erik Brunvand, Nick Michell, and Steven M. Nowick, "A Correctness Criterion for Asynchronous Circuit Validation and Optimization," *IEEE Transactions on Computer Aided Design*, Vol.13, No.11, November 1994, pp. 1309-1318.

29. Ganesh Gopalakrishnan and Venkatesh Akella, "High Level Optimizations in Compiling Process Descriptions to Asynchronous Circuits," *Journal of VLSI Signal Processing* (Kluwer), No. 7, 1994, pp. 33-45.
30. Ganesh Gopalakrishnan and Richard Fujimoto, "Design and Verification of the Rollback Chip using HOP: An Illustration of Formal Methods Applied to Hardware Design," *ACM Transactions on Computer Systems (TOCS)*, Vol.11, No.2, May 1993, pp. 109-145.
31. Ganesh Gopalakrishnan and Venkatesh Akella, "VLSI Asynchronous Systems: Specification and Synthesis," *Microprocessors & Microsystems*, Vol.16, No.10, October 1992, pp. 517-527.
32. Richard M. Fujimoto, Jya-jang Tsai, and Ganesh Gopalakrishnan, "Design and Evaluation of the Rollback Chip: Special Purpose Hardware for Time Warp," *IEEE Trans. on Computer*, Vol.41, No.1, 1992, pp. 68-82.
33. Ganesh C. Gopalakrishnan, Richard Fujimoto, Venkatesh Akella, and Narayana Mani, "HOP: A Process Model for Synchronous Hardware. Semantics, and Experiments in Process Composition," *Integration: The VLSI Journal* (North-Holland), 8 (1989), pp. 209-247.
34. Ganesh C. Gopalakrishnan and Mandayam K. Srivas, "Implementing Functional Programs Using Mutable Abstract Data Types," *Information Processing Letters*, Vol.26, No.6, Jan 1988.

CONFERENCE/WORKSHOP PAPERS: PRIOR TO 2017

2016

1. A.F. Donaldson, G. Gopalakrishnan, N. Chong, J. Ketema, G. Li, P. Li, A. Lokhmotov, S. Qadeer, "Formal analysis techniques for reliable GPU programming: current solutions and call to action," Chapter 1, *Advances in GPU Research and Practice by Hamid Sarbazi-Azad*, Released September 2016, Publisher(s): Morgan Kaufmann, ISBN: 9780128037881.
2. Simone Atzeni, Ganesh Gopalakrishnan, Zvonimir Rakamaric, Dong H. Ahn, Gregory L Lee, Ignacio Laguna, Martin Schulz, Joachim Protze, and Matthias Mueller, "ARCHER: Effectively Spotting Data Races in Large OpenMP Applications," IPDPS, May, 2016.
3. Sriram Aananthakrishnan, Greg Bronevetsky, Mark S. Baranowski, and Ganesh Gopalakrishnan, "ParFuse: Parallel and Compositional analysis of Message Passing Programs," The 29th International Workshop on Languages and Compilers for Parallel Computing (LCPC), September, 2016.
4. Tyler Sorenson, Alastair F. Donaldson, Mark Batty, Ganesh Gopalakrishnan, and Zvonimir Rakamaric, "Portable Inter-Workgroup Barrier Synchronisation for GPUs," Object-Oriented Programming, Systems, Languages & Applications (SPLASH), November, 2016.
5. Vishal Chandra Sharma, Ganesh Gopalakrishnan, and Sriram Krishnamoorthy, "PRESAGE: Protecting Structured Address Generation against Soft Errors," The 23rd annual IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC), December, 2016.
6. Vishal Chandra Sharma, Ganesh Gopalakrishnan, Sriram Krishnamoorthy, "Towards Resiliency Evaluation of Vector Programs," 21st IEEE Workshop on Dependable Parallel, Distributed and Network-Centric Systems (DPDNS) 2016.
7. Mohammed Al-Mahfoudh, Ganesh Gopalakrishnan, and Ryan Stutsman, "Toward Rigorous Design of Domain-Specific Distributed Systems," Workshop on Formal Methods in Software Engineering (FormaliSE) May, 2016.
8. Mohammed S. Al-Mahfoudh, Ganesh Gopalakrishnan, Ryan Stutsman, "Toward Bringing Distributed Systems Design upon Rigorous Footing," Workshop on Formal Methods and Integration (FMi). 2016.

2015

9. Charles Jacobsen, Alexey Solovyev, Ganesh Gopalakrishnan, "A Parametrized Floating-Point Formalization in HOL Light," *Electronic Notes in Theoretical Computer Science*, Vol-

ume 317, 18 November 2015, Pages 101–107, (selected from the papers presented at the Seventh and Eighth International Workshops on Numerical Software Verification, NSV). doi:10.1016/j.entcs.2015.10.010.

10. Wei-Fan Chiang, Ganesh Gopalakrishnan, and Zvonimir Rakamaric, “Unsafe Floating-point to Unsigned Integer Casting Check for GPU Programs,” NSV 2015, Seattle, WA.
 11. Alexey Solovyev, Charles Jacobsen, Zvonimir Rakamaric and Ganesh Gopalakrishnan, “Rigorous Estimation of Floating-Point Round-off Errors with Symbolic Taylor Expansions,” pp. 532-550, Nikolaj Bjørner and Frank S. de Boer (ed.), FM 2015, LNCS 9109.
 12. Jade Alglave, Mark Batty, Alastair F. Donaldson, Ganesh Gopalakrishnan, Jeroen Ketema, Daniel Poetzl, Tyler Sorensen and John Wickerson, “GPU concurrency: Weak behaviours and programming assumptions,” ASPLOS 2015, Istanbul, Turkey.
- 2014
13. Joachim Protze, Simone Atzeni, Dong H. Ahn, Martin Schulz, Ganesh Gopalakrishnan, Matthias S. Muller, Ignacio Laguna, Zvonimir Rakamaric, Greg L. Lee., “Towards Providing Low-Overhead Data Race Detection for Large OpenMP Applications,” LLVM Compiler Infrastructure in HPC Workshop (LLVM-HPC 2014), New Orleans, LA, USA.
 14. Diego Caminha B de Oliveira, Alan Humphrey, Qingyu Meng, Zvonimir Rakamaric, Martin Berzins and Ganesh Gopalakrishnan, “Systematic Debugging of Concurrent Systems Using Coalesced Stack Trace Graphs,” LCPC 2014.
 15. Peng Li, Guodong Li, and Ganesh Gopalakrishnan, “Practical Symbolic Checking of GPU Programs,” Supercomputing (SC 2014).
 16. Vishal Chandra Sharma, Zvonimir Rakamarić and Ganesh Gopalakrishnan, “FUSED: A Low-cost Online Soft-Error Detector,” 10th Workshop on Silicon Errors in Logic - System Effects (SELSE) 2014.
 17. Wei-Fan Chiang, Ganesh Gopalakrishnan, Zvonimir Rakamaric and Alexey Solovyev, “Efficient Search for Inputs Causing High Floating-point Errors,” Principles and Practices of Parallel Programming (PPoPP), February, 2014.

2013

18. Vishal Chandra Sharma, Arvind Haran, Zvonimir Rakamarić, and Ganesh Gopalakrishnan, “Towards Formal Approaches to System Resilience,” 19th IEEE Pacific Rim International Symposium on Dependable Computing (PRDC) 2013.
19. Wei-Fan Chiang, Ganesh Gopalakrishnan, Guodong Li and Zvonimir Rakamarić, *Formal Analysis of GPU Programs with Atomics via Conflict-Directed Delay-Bounding*, NASA Formal Methods Conference, May 2013.
20. Diego Caminha B. de Oliveira, Zvonimir Rakamarić, Ganesh Gopalakrishnan, Alan Humphrey, Qingyu Meng and Martin Berzins, *Crash Early, Crash Often, Explain Well: Practical Formal Correctness Checking of Million-core Problem Solving Environments for HPC*, Software Engineering for Computational Science and Engineering, May 2013.
21. Wei-Fan Chiang, Ganesh Gopalakrishnan, Zvonimir Rakamaric, Dong H. Ahn and Gregory L. Lee, *Determinism and Reproducibility in Large-Scale HPC Systems*, March 2013. <http://wodet.cs.washington.edu/workshop-program/>
22. Sriram Ananthakrishnan, Greg Bronevetsky, and Ganesh Gopalakrishnan, “Hybrid Approach for Data-flow Analysis of MPI Programs,” Proceedings of the 27th international ACM conference on International Conference on Supercomputing, 2013.
23. Tyler Sorensen, Ganesh Gopalakrishnan, and Vinod Grover, “Towards Shared Memory Consistency Models for GPUs,” Proceedings of the 27th international ACM conference on International conference on supercomputing, 2013.

2012

24. Guodong Li and Ganesh Gopalakrishnan, "Parameterized Verification of GPU Kernels," PLC Workshop 2012 (An IPDPS 2012 Workshop)
25. Ganesh Gopalakrishnan, "Formal Methods for Surviving the Jungle of Heterogeneous Parallelism," EduPar (An IPDPS 2012 Workshop)
26. Ganesh Gopalakrishnan and Tyler Sorensen, "Integrating Formal Methods for Parallelism and Concurrency into Existing CS Curricula," EduPar Poster (An IPDPS 2012 Workshop)
27. Peng Li, Guodong Li, and Ganesh Gopalakrishnan, "Parametric Flows: Automated Behavior Equivalencing for Symbolic Analysis of Races in CUDA Programs," Supercomputing 2012, Salt Lake City, UT, November 2012.
28. Subodh Sharma, Ganesh Gopalakrishnan, and Greg Bronevetsky, "A Sound Reduction of Persistent-sets for Deadlock Detection in MPI Applications," SMBF 2012 - The Brazilian Symposium on Formal Methods, Natal, September 2012.
29. Guodong Li, Peng Li, Geof Sawaya, Ganesh Gopalakrishnan, Indradeep Ghosh, and Sreeranga P. Rajan, "GKLEE: Concolic Verification and Test Generation for GPUs," Principles and Practices of Parallel Programming (PPoPP), February, 2012.

2011

30. Anh Vo, Ganesh Gopalakrishnan, Robert M. Kirby, Bronis R. de Supinski, Martin Schulz, and Greg Bronevetsky, "Large Scale Verification of MPI Programs Using Lamport Clocks with Lazy Update," Parallel Architectures and Compilation Techniques (PACT), Galveston, TX, October 2011.
31. Stephen F. Siegel and Ganesh Gopalakrishnan, "Formal Analysis of Message Passing," Invited Tutorial Paper, pages 2-18, Verification, Model Checking and Abstract Interpretation 2011, Austin, TX.
32. Caitlin Sadowski, Thomas Ball, Judith Bishop, Sebastian Burckhardt, Ganesh Gopalakrishnan, Joseph Mayo, Madanlal Musuvathi, Shaz Qadeer, and Stephen Toub, "Practical Parallel and Concurrent Programming," ACM SIGCSE, Waikiki, May 2011.

2010

33. Ganesh L. Gopalakrishnan and Robert M. Kirby, Top Ten Ways to make Formal Methods for HPC Practical, 2010 FSE/SDP Workshop on the Future of Software Engineering Research, Santa Fe, NM, November, ACM, http://www.cs.utah.edu/formal_verification/pdf/sdp2010-workshop.pdf, 2010.
34. Anh Vo, Sriram Ananthakrishnan, Ganesh Gopalakrishnan, Bronis R. de Supinski, Martin Schulz, and Greg Bronevetsky, "A Scalable and Distributed Dynamic Formal Verifier for MPI Programs," Supercomputing 2010, New Orleans, LA.
<http://www.computer.org/portal/web/csdl/doi/10.1109/SC.2010.7>
35. Sarvani Vakkalanka, Anh Vo, Ganesh Gopalakrishnan, and Robert Kirby, "Precise Dynamic Analysis for Slack Elasticity: Adding Buffer Without Adding Bugs," Recent Advances in the Message Passing Interface, 17th European MPI Users' Group Meeting, EuroMPI 2010, September 2010, LNCS 6305, 152-159, Stuttgart, Germany.
36. Wei-Fan Chiang, Grzegorz Szubzda, Ganesh Gopalakrishnan, and Rajeev Thakur, "Dynamic Verification of Hybrid Programs," EuroMPI, 2010, LNCS 6305, 298-301, Stuttgart, Germany.
37. Alan Humphrey, Christopher Derrick, Ganesh Gopalakrishnan, and Beth R. Tibbitts, "GEM: Graphical Explorer for MPI Programs," Parallel Software Tools and Tool Infrastructures (ICPP workshop), <http://www.cs.utah.edu/fv/GEM>, 2010.
38. Guodong Li and Ganesh Gopalakrishnan, Scalable SMT-based verification of GPU kernel functions, Foundations of Software Engineering, 2010, <http://www.cs.utah.edu/fv/PUG>, 187-

196.

39. Anh Vo, Ganesh Gopalakrishnan, Sarvani Vakkalanka, Alan Humphrey and Christopher Derrick, "Seamless Integration of Two Approaches to Dynamic Formal Verification of MPI Programs," Workshop on Advances in Message Passing, 2010.
40. Guodong Li, Ganesh Gopalakrishnan, Robert M. Kirby, Dan Quinlan, "A symbolic verifier for CUDA programs," PPOPP 2010: 357-358.

2009

41. Sarvani S. Vakkalanka, Anh Vo, Ganesh Gopalakrishnan, Robert M. Kirby, "Reduced Execution Semantics of MPI: From Theory to Practice," FM 2009: 724-740.
42. Subodh Sharma, Ganesh Gopalakrishnan, Eric Mercer, Jim Holt, "MCC: A runtime verification tool for MCAPI user applications," FMCAD 2009: 41-44.
43. Subodh Sharma, Todd Dukes and Ganesh Gopalakrishnan, "Symbolic Execution Engine to Explore Path Feasibility in Assembly Programs," Microprocessor Test and Verification (MTV'09), Austin, TX, December 2009.
44. Subodh Sharma, Ganesh Gopalakrishnan, and Eric Mercer, "Dynamic Verification of Multi-core Communication Applications in MCAPI," HLDVT 2009, November, San Francisco, CA.
45. Ganesh Gopalakrishnan, Yu Yang, Sarvani S. Vakkalanka, Anh Vo, Sriram Aananthakrishnan, Grzegorz Szubzda, Geoffrey Sawaya, Jason Williams, Subodh Sharma, Michael Delisi, Simone Atzeni, "Some resources for teaching concurrency," PADTAD 2009.
46. Anh Vo, Sarvani S. Vakkalanka, Michael Delisi, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, "Formal verification of practical MPI programs," PPOPP 2009: 261-270.
47. Sriram Aananthakrishnan, Michael Delisi, Sarvani S. Vakkalanka, Anh Vo, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, "How Formal Dynamic Verification Tools Facilitate Novel Concurrency Visualizations," PVM/MPI 2009: 261-270.
48. Anh Vo, Sarvani S. Vakkalanka, Jason Williams, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, "Sound and Efficient Dynamic Verification of MPI Programs with Probe Non-determinism," PVM/MPI 2009: 271-281.
49. Sarvani S. Vakkalanka, Grzegorz Szubzda, Anh Vo, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, "Static-Analysis Assisted Dynamic Verification of MPI Waitany Programs (Poster Abstract)," PVM/MPI 2009: 329-330.
50. Ganesh Gopalakrishnan, Robert M. Kirby, "Practical Formal Verification of MPI and Thread Programs," PVM/MPI 2009: 8 (Tutorial abstract)
51. Yu Yang, Xiaofang Chen, Ganesh Gopalakrishnan, Chao Wang, "Automatic Discovery of Transition Symmetry in Multithreaded Programs Using Dynamic Analysis," SPIN 2009: 279-295.

2008

52. Chao Wang, Yu Yang, Aarti Gupta, and Ganesh Gopalakrishnan, "Dynamic Model Checking with Property Driven Pruning to Detect Race Conditions," ATVA 2008, pp. 126-140, LNCS 5311.
53. Ganesh Gopalakrishnan, Robert M. Kirby, "Runtime verification methods for MPI," IPDPS 2008: 1-5.
54. Sarvani Vakkalanka, Michael DeLisi, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, and William Gropp, "Implementing Efficient Dynamic Formal Verification Methods for MPI Programs," Recent Advances in Parallel Virtual Machine and Message Passing Interface (EuroPVM/MPI), Dublin, Ireland, 2008, LNCS 5205, pp. 248-256.
55. Subodh Sharma, Sarvani Vakkalanka, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, and William Gropp, "A Formal Approach to Detect Functionally Irrelevant Barri-

- ers in MPI Programs,” Recent Advances in Parallel Virtual Machine and Message Passing Interface (EuroPVM/MPI), Dublin, Ireland, 2008, LNCS 5205, pp. 265-273.
56. Yu Yang, Xiaofang Chen, Ganesh Gopalakrishnan, and Robert M. Kirby, “Efficient Stateful Dynamic Partial Order Reduction,” Model Checking Software, 15th International SPIN Workshop, Los Angeles, CA, August 2008, LNCS , pp. 288-305.
 57. Sarvani Vakkalanka, Michael DeLisi, Ganesh Gopalakrishnan, and Robert M. Kirby, “Scheduling Considerations for Building Dynamic Verification Tools for MPI,” Parallel and Distributed Systems - Testing and Debugging (PADTAD-VI), Seattle, WA, July, 2008.
 58. Sarvani Vakkalanka, Michael DeLisi, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, and William Gropp, “Implementing Efficient Dynamic Formal Verification Methods for MPI Programs,” Recent Advances in Parallel Virtual Machine and Message Passing Interface (EuroPVM/MPI), Dublin, Ireland, 2008, LNCS 5205, pp. 248-256.
 59. Subodh Sharma, Sarvani Vakkalanka, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, and William Gropp, “ A Formal Approach to Detect Functionally Irrelevant Barriers in MPI Programs,” Recent Advances in Parallel Virtual Machine and Message Passing Interface (EuroPVM/MPI), Dublin, Ireland, 2008, LNCS 5205, pp. 265-273.
 60. Sarvani Vakkalanka, Ganesh Gopalakrishnan, and Robert M. Kirby, “Dynamic Verification of MPI Programs with Reductions in Presence of Split Operations and Relaxed Orderings,” Computer Aided Verification (CAV 2008), pp. 66-79, LNCS 5123.
 61. Guodong Li, Michael DeLisi, Ganesh Gopalakrishnan, and Robert M. Kirby, “Formal Specification of the MPI-2.0 Standard in TLA+,” Poster Paper, Principles and Practices of Parallel Programming (PPoPP), 283-284, 2008.
 62. Sarvani Vakkalanka, Subodh V. Sharma, Ganesh Gopalakrishnan, and Robert M. Kirby, “ISP: A Tool for Model Checking MPI Programs,” Poster Paper, Principles and Practices of Parallel Programming (PPoPP), 285-286, 2008.

2007

63. Ganesh Gopalakrishnan and Robert M. Kirby, “Formal Methods for MPI Programs,” Pages 19-27, Issue 193, Electronic Notes in Theoretical Computer Science (ENTCS), 2007.
64. Salman Pervez, Robert Palmer, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, and William Gropp, “Practical Model Checking Methods for Verifying Correctness of MPI Programs,” Recent Advances in Parallel Virtual Machine and Message Passing Interface (EuroPVM/MPI), Paris, 344–353, LNCS 4757, France, September 30 - October 3, 2007.
65. Robert Palmer, Ganesh Gopalakrishnan and Robert M. Kirby, “Semantics Driven Dynamic Partial-Order Reduction of MPI-based Parallel Programs,” Proceedings of Parallel and Distributed Systems: Testing and Debugging (PADTAD), London, England, July 9, 2007. Won the Best Paper award.
66. Robert Palmer, Michael DeLisi, Ganesh Gopalakrishnan and Robert M. Kirby, “An Approach to Formalization and Analysis of Message Passing Libraries,” Proceedings of the 12th International Workshop on Formal Methods for Industrial Critical Systems (FMICS), Berlin, Germany, July 1-2, 2007. Won the EASST (European Association of Software Science and Technology) Best Paper Award.
67. Yu Yang, Xiaofang Chen, Ganesh Gopalakrishnan and Robert M. Kirby, “Distributed Dynamic Partial Order Reduction Based Verification of Threaded Software,” Proceedings of Model Checking Software: 14th International SPIN Workshop, Berlin, Germany, July 1-3, 2007.
68. Xiaofang Chen, Steven M. German, and Ganesh Gopalakrishnan, “Transaction Based Modeling and Verification of Hardware Protocols,” Formal Methods in Computer Aided Design, Austin, November 11-14, 2007, pages 53-61.

69. Xiaofang Chen, Steven M. German and Ganesh Gopalakrishnan, "Transaction Based Modeling and Verification of Hardware Protocols," TECHCON, Lake Buena Vista, FL, 2007. Best Paper in Verification Session.
70. Xiaofang Chen, Yue Yang, Michael Delisi, Ganesh Gopalakrishnan, Ching-Tsun Chou, "Hierarchical Cache Coherence Protocol Verification One Level at a Time through Assume Guarantee," IEEE Intl. High Level Design Validation and Test Workshop, Irvine, CA, Nov 7-9, 2007, pages 107-114.

2006

71. Robert Palmer, Ganesh Gopalakrishnan and Mike Kirby, "Formal Specification and Verification Using +CAL: An Experience Report," Verify'06 workshop (Post FLoC 2006), Seattle, Aug 15, 2006.
72. Xiaofang Chen, Yu Yang, Ganesh Gopalakrishnan, and Ching-Tsun Chou, "Reducing Verification Complexity of a Multicore Coherence Protocol Using Assume/Guarantee," Formal Methods in Computer Aided Design (FMCAD), IEEE, San Jose, Nov 11-16, 81-88, 2006.
73. Salman Pervez, Ganesh Gopalakrishnan, Robert M. Kirby, Rajeev Thakur, and William Gropp, "Formal Verification of Programs that use MPI One-sided Communication," Outstanding Paper, Recent Advances in Parallel Virtual Machine and Message Passing Interface (EuroPVM/MPI), Bonn, Germany, 2006, LNCS 4192, 30-39.
74. I. Melatti, R. Palmer, G. Sawaya, Y. Yang, R. M. Kirby, and G. Gopalakrishnan, "Parallel and Distributed Model Checking in Eddy," Model Checking Software (13th International SPIN Workshop), Vienna, Austria, 2006, LNCS 3925, 108-125.
75. Ritwik Bhattacharya, Steven M. German, and Ganesh Gopalakrishnan, "Exploiting Symmetry and Transactions for Partial Order Reduction of Rule Based Specifications," Model Checking Software (13th International SPIN Workshop), Vienna, Austria, 2006, LNCS 3925, 252-270.

2005

76. Sudhindra Pandav, Konrad Slind, and Ganesh Gopalakrishnan, "Counterexample Guided Invariant Discovery for Parameterized Cache Coherence Verification," CHARME 2005, LNCS 2144, 317-331.
77. Ritwik Bhattacharya, Steven M. German, and Ganesh Gopalakrishnan, "Symbolic Partial Order Reduction for Rule Based Transition Systems," CHARME 2005, LNCS 2144, 332-335.
78. Ali Sezgin and Ganesh Gopalakrishnan, "On the decidability of shared memory consistency verification," Fourth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), 2005, 199-208.
79. Robert Palmer, Steve Barrus, Yu Yang, Ganesh Gopalakrishnan, and Robert M. Kirby, "Gauss: A Framework for Verifying Scientific Computing Software," Electronic Notes on Theoretical Computer Science (ENTCS), Vol. 144, No. 3, February 2006, 95-106.
80. Ganesh Gopalakrishnan and Robert M. Kirby, "Toward Reliable and Efficient Message Passing Software Through Formal Analysis," An IPDPS 2006 workshop on Next-Generation Systems, 2006, Athens, Greece. Organizer: Frederica Darema (NSF).

2004

81. Yue Yang, Ganesh Gopalakrishnan, and Gary Lindstrom, "Memory-Model-Sensitive Data Race Analysis," International Conference on Formal Engineering Methods (ICFEM), 2004, pages 30-45.
82. Yue Yang, Ganesh Gopalakrishnan, Gary Lindstrom, and Konrad Slind, "Nemos: A Framework for Axiomatic and Executable Specifications of Memory Consistency Models," Interna-

tional Parallel and Distributed Processing Symposium, 2004.

83. Ganesh Gopalakrishnan, Yue Yang, and Hemanthkumar Sivaraj, "QB or not QB: An Efficient Execution Verification Tool for Memory Orderings," Computer Aided Verification (CAV 2004), pp. 401-413, LNCS 3114.
84. Yue Yang, Ganesh Gopalakrishnan, Gary Lindstrom, and Konrad Slind, "Analyzing the Intel Itanium Memory Ordering Rules Using Logic Programming and SAT," Correct Hardware Design and Verification Methods, LNCS 2860, L'Aquila, Italy, pp. 81-95.

2003

85. Hemanthkumar Sivaraj and Ganesh Gopalakrishnan, "Random Walk Based Heuristic Algorithms for Distributed Memory Model Checking," 2nd International Workshop on Parallel and Distributed Model Checking (PDMC'03), Boulder, Colorado, USA, July 2003.
86. Yue Yang, Ganesh Gopalakrishnan, Gary Lindstrom, and Konrad Slind, "Analyzing the Intel Itanium Memory Ordering Rules Using Logic Programming and SAT," Correct Hardware Design and Verification Methods, LNCS 2860, L'Aquila, Italy, pp. 81-95, 2003.

2002

87. Yue Yang, Ganesh Gopalakrishnan, and Gary Lindstrom, "Specifying Java Thread Semantics using a Uniform Memory Model," Joint ACM Java Grande - ISCOPE Conference, pp.192-201, ISBN:1-58113-599-8, 2002.
88. Robert Palmer and Ganesh Gopalakrishnan, "The Parallel PV Model-Checker," International Workshop on Parallel and Distributed Model Checking (PDMC'02), Brno, Czech Republic, August, 2002.
89. Prosenjit Chatterjee, Hemanthkumar Sivaraj, and Ganesh Gopalakrishnan, "Shared memory consistency protocol verification against weak memory models: refinement via distributed model-checking." 14th International Conference on Computer Aided Verification, Copenhagen, July 2002.
90. Ritwik Bhattacharya and Ganesh Gopalakrishnan, "Issues in Multiprocessor Memory Consistency Protocol Design and Verification." Workshop on Designing Correct Circuits (DCC), Grenoble, France, August 2002.
91. Michael Jones and Ganesh Gopalakrishnan, "Verifying Parameterized Input/Output Networks Through Partial-Concretization Based Reachability Analysis," to be submitted to Formal Methods in Computer-Aided Design (FMCAD) 2002.
92. Annette Bunker, Sally A. McKee, and Ganesh Gopalakrishnan. "An Overview of Formal Hardware Specification Languages." Grace Hopper Celebration of Women in Computing, October 2002.
93. A. Weinzoepflen, M.D. Jones, D. Mery, D. Cansel and G. Gopalakrishnan, "Incremental Proof of the Producer/Consumer Property for the PCI Protocol," ZB2002: Formal Specification and Development in Z and B, Grenoble, France, January 2002. Springer LNCS v.2272, pages 22-42.

2001

94. Annette Bunker and Ganesh Gopalakrishnan. "Using Live Sequence Charts for Hardware Protocol Specification and Compliance Verification," in IEEE International High Level Design Validation and Test Workshop. IEEE Computer Society Press, November 2001, pages 95-100.
95. Annette Bunker and Ganesh Gopalakrishnan, "An Approach to the Specification and Verification of System-on-Chip Compliance to Interfacing Standards," International Conference on Integrated Design and Process Technology (IDPT), Pasadena, June 2002.
96. Jason Yang, Ganesh Gopalakrishnan, and Gary Lindstrom, "Analyzing the CRF Java Mem-

- ory Model with Murphi,” Workshop on Software Model-checking, Paris, France, July 2001.
97. Jason Yang, Ganesh Gopalakrishnan, and Gary Lindstrom, “Analyzing the CRF Java Memory Model with Murphi,” *Asia Pacific Software Engineering Conference*. Macau, 2001.
 98. Prosenjit Chatterjee and Ganesh Gopalakrishnan, “Towards a Formal Model of Shared Memory Consistency for Intel Itanium,” International Conference on Computer Design, Austin, TX, October 2001, 515-518.

2000

99. Michael Jones and Ganesh Gopalakrishnan, “Verifying Transaction Ordering Properties in Unbounded Multi-Bus Networks through Algorithmic and Deductive Methods,” Formal Methods in Computer-Aided Design 2000 FMCAD’00), Austin, Texas.
100. Hans Jacobson, Chris Myers, and Ganesh Gopalakrishnan, “Achieving Fast and Exact Hazard-Free Logic Minimization of Extended Burst-Mode gC Finite State Machines,” ICCAD, November, 2000.
101. Ravi Hosabettu, Ganesh Gopalakrishnan, and Mandayam Srivas, “Verifying Microarchitectures that Support Speculation and Exceptions,” Computer Aided Verification (CAV), Springer-Verlag LNCS 1855, 12th International Conference, Chicago, IL, July, 2000, pp. 521-537.
102. Rajnish Ghughal and Ganesh Gopalakrishnan, “Verification methods for weaker shared memory consistency models,” Proceedings of the workshop FMPPTA (Formal Methods for Parallel Programming: Theory and Applications), Cancun, Mexico, May, 2000. Lecture Notes in Computer Science # 1800, José Rolim et al. (Eds.), pages 985-992.
103. Hans Jacobson, Erik Brunvand, Ganesh Gopalakrishnan, and Prabkaha Kudva, “High Level Asynchronous System Design Using the ACK Framework,” in Async’00, Proc. Sixth International Symposium on Advanced Research in Asynchronous Circuits and Systems, Eilat, Israel, April, 2000. IEEE Computer Society, ISBN 0-7695-0586-4, pages 93-103.

1999

104. Ravi Hosabettu, Ganesh Gopalakrishnan, and Mandayam Srivas, “A Proof of Correctness of a Processor Implementing Tomasulo’s Algorithm Without a Reorder Buffer,” IFIP TC 10 WG 10.5 International Conference on Correct Hardware and Verification Methods (Charme’99), Bad Herrenalb (Germany), September 27-29, 1999. pp. 8-22, Springer LNCS.
105. Ravi Hosabettu, Mandayam Srivas, and Ganesh Gopalakrishnan, “Proof of Correctness of a Processor with Reorder Buffer using the Completion Functions Approach,” Computer Aided Verification, 11th International Conference, CAV’99, Trento, Italy, July 7-10, 1999. pp. 47-59.

1998

106. Ratan Nalumasu and Ganesh Gopalakrishnan, “PV: an Explicit Enumeration Model-checker,” Formal Methods in Computer Aided Design, Second International Conference, FMCAD’98, Palo Alto, CA, USA, Nov 1998, Proceedings. Ganesh Gopalakrishnan and Phillip Windley (editors). Springer-Verlag LNCS 1522. pp. 523-528.
107. Abdel Mokkedem, Ravi Hosabettu, and Ganesh Gopalakrishnan, “Formalization and Proof of a Solution to the PCI 2.1 Bus Transaction Ordering Problem,” Formal Methods in Computer Aided Design, Second International Conference, FMCAD’98, Palo Alto, CA, USA, Nov 1998, Proceedings. Ganesh Gopalakrishnan and Phillip Windley (editors). Springer-Verlag LNCS 1522. pp. 237-254.
108. Ratan Nalumasu, Rajnish Ghughal, Abdel Mokkedem, and Ganesh Gopalakrishnan, “The ‘Test Model-checking’ Approach to the Verification of Formal Memory Models of Multiprocessors,” Computer Aided Verification, 10th International Conference, CAV’98, Vancouver,

- B.C., Canada, June/July 1998, Proceedings. Alan J. Hu and Moshe Y. Vardi (editors). Springer-Verlag LNCS 1427. pp. 464-476.
109. Ravi Hosabettu, Mandayam Srivas, and Ganesh Gopalakrishnan, "Decomposing the Proof of Correctness of Pipelined Microprocessors," Computer Aided Verification, 10th International Conference, CAV'98, Vancouver, B.C., Canada, June/July 1998, Proceedings. Alan J. Hu and Moshe Y. Vardi (editors). Springer-Verlag LNCS 1427. pp. 122-134.
 110. Rajnish Ghughal, Abdel Mokkedem, Ratan Nalumasu, and Ganesh Gopalakrishnan, "Using 'Test Model-Checking' to Verify the Runway-PA800 Memory Model," SPAA'98, Tenth Annual ACM Symposium on Parallel Algorithms and Architectures, Puerto Vallarta, Mexico, June 28-July 2, 1998. pp. 231-239.
 111. Ratan Nalumasu and Ganesh Gopalakrishnan, "Deriving Efficient Cache Coherence Protocols Through Refinement," Formal Methods for Parallel Programming: Theory and Applications (FMPPTA'98), April 1998.

1997

112. Ganesh Gopalakrishnan, Rajnish Ghughal, Ravi Hosabettu, Abdel Mokkedem, and Ratan Nalumasu, "Formal Modeling and Validation Applied to a Commercial Coherent Bus: A Case Study," Proceedings of CHARME (Correct Hardware design Methods), Montreal, October, 1997, pp. 48-64.
113. Hans Jacobson and Ganesh Gopalakrishnan, "Asynchronous Microengines for Efficient High-level Control," Advanced Research on VLSI (ARVLSI'97), Michigan, September 1997, pp. 201-218.
114. Ratan Nalumasu and Ganesh Gopalakrishnan, "PV: A Model-checker for Verifying LTL-X Properties," Lfm97: Fourth NASA LaRC Formal Methods Workshop, 10-12 September 1997, Hampton, Virginia.
115. Ratan Nalumasu and Ganesh Gopalakrishnan, "A New Partial Order Reduction Algorithm for Concurrent System Verification," Proceedings of the 1997 Computer Hardware Description Languages, Toledo, Spain, April 1997, pp. 305-314.

1996

116. Prabhakar Kudva, Ganesh Gopalakrishnan, and Hans Jacobson, "A Technique for Synthesizing Distributed Burst-mode Circuits," ACM 33rd Design Automation Conference (DAC'96), Las Vegas, NV, June 3-8, 1996, pp. 67-70.
117. Prabhakar Kudva, Hans Jacobson, Ganesh Gopalakrishnan, and Steven M. Nowick, "Synthesis of Hazard-free Customized CMOS Complex-gate Networks under Multiple-input Changes," ACM 33rd Design Automation Conference (DAC'96), Las Vegas, NV, June 3-8, 1996, pp. 77-82.

1995

118. Prabhakar Kudva and Ganesh Gopalakrishnan, "Techniques for Synthesizing Efficient Burst-mode Circuits," In TAU, workshop on Timing Issues in the Specification and Synthesis of Digital Systems, Seattle, WA, Nov 10-11, 1995.
119. Prabhakar Kudva, Ganesh Gopalakrishnan, and Venkatesh Akella, "An Asynchronous High Level Synthesis System Targeted at Interacting Burst-Mode Controllers," Proceedings of the 1995 Computer Hardware Description Languages, Chiba, Japan, August, 1995, pp. 605-610.
120. Ratan Nalumasu and Ganesh Gopalakrishnan, "Explicit-enumeration based Verification made Memory-efficient," Proceedings of the 1995 Computer Hardware Description Languages, Chiba, Japan, August, 1995, pp. 617-622.
121. Jae-Tack Yoo, Ganesh Gopalakrishnan, Kent Smith, and John Mathews, "Counterflow-

Clocked Pipelining Illustrated on the Design of High Speed HDTV Subband Vector Quantizer Chips,” Advanced Research on VLSI (ARVLSI’95), Chapel Hill, March 1995. (16 pages.)

1994

122. Prabhakar Kudva, Ganesh Gopalakrishnan, and Erik Brunvand, “Performance Analysis and Optimization of Asynchronous Circuits,” Intl. Conference on Computer Design (ICCD), 1994, pp. 221-224.
123. Ganesh Gopalakrishnan, Prabhakar Kudva, Erik Brunvand, and Venkatesh Akella, “Peep-hole Optimization of Asynchronous Networks through Process Composition and Burst-mode Machine Generation,” Intl. Conference on Computer Design (ICCD), 1994, pp. 442-446.
124. Ganesh Gopalakrishnan and Lüli Josephson, “Towards Amalgamating the Synchronous and Asynchronous Design Styles,” TAU ’93, Timing Aspects of VLSI, Malente, Germany. (13 pages.)

1993

125. Ganesh Gopalakrishnan and Venkatesh Akella, “A Transformational Approach to Asynchronous High-level Synthesis,” VLSI ’93, Grenoble, France, September 1993. IFIP/North-Holland publishers. pp. 201-210.

1992

126. John Hurdle, Lüli Josephson, Erik Brunvand, and Ganesh Gopalakrishnan, “Asynchronous Models for Large Scale Neurocomputing Applications,” ‘NEURO NIMES ’92: Fifth International Conference on Neural Networks & their Applications,’ November 2-6, 1992, Nimes, France.
127. Venkatesh Akella and Ganesh Gopalakrishnan, “SHILPA: A High-level Synthesis System for Self-Timed Circuits,” accepted for publication in the International Conference on Computer Aided Design (ICCAD’92), Santa Clara, Nov. 1992. pp. 587-594.
128. Armin Liebchen and Ganesh Gopalakrishnan. “Dynamic Reordering of High Latency Transactions in Time-Warp Simulation Using a Modified Micropipeline,” *International Conference on Computer Design (ICCD) 1992*, pp. 336-340.
129. Prabhat Jain and Ganesh Gopalakrishnan. “Efficient Symbolic Simulation Based Verification Using the Parametric form of Boolean Expressions,” *International Conference on Computer Design (ICCD) 1992*, pp. 598-602.
130. Prabhat Jain, Prabhakar Kudva, and Ganesh Gopalakrishnan, “Towards a Verification Technique for Large Synchronous Circuits,” The Fourth Computer-Aided Verification Workshop (CAV’92), Montreal, June 1992.
131. Venkatesh Akella and Ganesh Gopalakrishnan. “Flow Analysis Techniques for the Synthesis of Efficient Asynchronous Circuits,” *In TAU ’92: 1992 Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, Princeton, NJ, March 18–20, 1992.*

1991

132. Venkatesh Akella and Ganesh Gopalakrishnan, “Hierarchical Action Refinement: A Methodology for Compiling Asynchronous Circuits from a Concurrent HDL,” Proceedings of the Tenth International Symposium on Computer Hardware Description Languages and their Applications, Marseille, France, April 1991.
133. Ganesh Gopalakrishnan and Prabhat Jain and Venkatesh Akella and Lüli Josephson and Wen-Yan Kuo, “Combining Verification and Simulation,” Advanced Research in VLSI (ARVLSI’91), Proceedings of the 1991 University of California Santa Cruz Conference, The MIT Press, 1991, Carlo Sequin (Ed.), pp. 323-339.

134. Ganesh Gopalakrishnan and Prabhat Jain, "A Practical Approach to Synchronous Hardware Verification," in VLSI Design '91: The Fourth CSI/IEEE International Symposium on VLSI Design, January 5-8, 1991, New Delhi, India.

1990

135. Venkatesh Akella and Ganesh Gopalakrishnan, "High Level Test Generation via Process Composition," Designing Correct Circuits, Oxford, 1990, Springer Verlag, Proceedings of the DCC Workshop, Oxford, September, 1990, Published in Springer series 'Workshops in Computing,' pp. 99-119

1989

136. Ganesh C. Gopalakrishnan, Narayana Mani, and Venkatesh Akella, "A Design Validation System for Synchronous Hardware based on a Process Model: A Case Study," IMEC-IFIP Workshop on 'Applied Formal Methods for Correct VLSI Design,' Nov. 13-16, Leuven, Belgium, 1989. pp. 227-246.
137. Ganesh C. Gopalakrishnan, Richard M. Fujimoto, Venkatesh Akella, N.S. Mani, and Kevin Smith, "Specification Driven Design of Custom VLSI Architectures in HOP," G. Birtwistle and P.A. Subrahmanyam (editors), *Current Trends in Hardware Verification and Automated Theorem Proving*, Chapter 3, pp. 128-170, Springer-Verlag, 1989.
138. Ganesh C. Gopalakrishnan, "Specification and Verification of Pipelined Hardware in HOP," Ninth International Symposium on Computer Hardware Description Languages (CHDL'89), Washington, D.C., June, 1989, pp. 117-131.
139. Ganesh C. Gopalakrishnan, Narayana Mani, and Venkatesh Akella, "Parallel Composition of Lock-step Synchronous Processes for Hardware Validation: Divide-and-conquer Composition," in Springer Verlag Lecture Notes in Computer Science, No.407 (*Automatic Verification Methods for Finite-State Systems*, International Workshop, Grenoble, France, June 1989), J.Sifakis (Editor), pp. 374-382.

1988

140. Richard M. Fujimoto, Jya-Jang Tsai and Ganesh C. Gopalakrishnan, "Design and Performance Evaluation of the Roll Back Chip," 1988 IEEE/ACM Computer Architecture Conference (ISCA'88), Honolulu, Hawaii, June 1988. pp. 401-408.
141. Richard M. Fujimoto, Jya-Jang Tsai and Ganesh C. Gopalakrishnan, "The Roll Back Chip: Hardware Support for Distributed Simulation Using Time Warp," the Society for Computer Simulation Multiconference, San Diego, CA, Feb 1988.

1987

142. Ganesh C. Gopalakrishnan, "Synthesizing Synchronous Digital VLSI Controllers Using Petri Nets," Internal Workshop on Petri Nets and Performance Models, Wisconsin, August 24-26 (1987).
143. Ganesh C. Gopalakrishnan, M.K. Srivas, and D.R. Smith, "From Algebraic Specifications to Correct VLSI Circuits," in book *From HDL Descriptions to Guaranteed Correct Circuit Designs*, D. Borrione (Ed.), IFIP, North-Holland (1987) 197-225.

1986

144. Ganesh C. Gopalakrishnan, N.C.Lee, D.R.Smith and M.K.Srivas, "Deriving Module Interconnectivity From Behavioral Specifications and Coupling a VLSI Layout Editor for Error-free Routing," 1986 Fall Joint Computer Conference, Dallas, Nov. 1986.

1985

145. Ganesh C. Gopalakrishnan, D.R.Smith, and M.K.Srivas, "An Algebraic Approach to the Specification and Realization of VLSI Designs," 7th International Symposium on Computer Hardware Description Languages (CHDL'85), Tokyo, Japan, Aug. 1985, North-Holland (1985) 16-38.